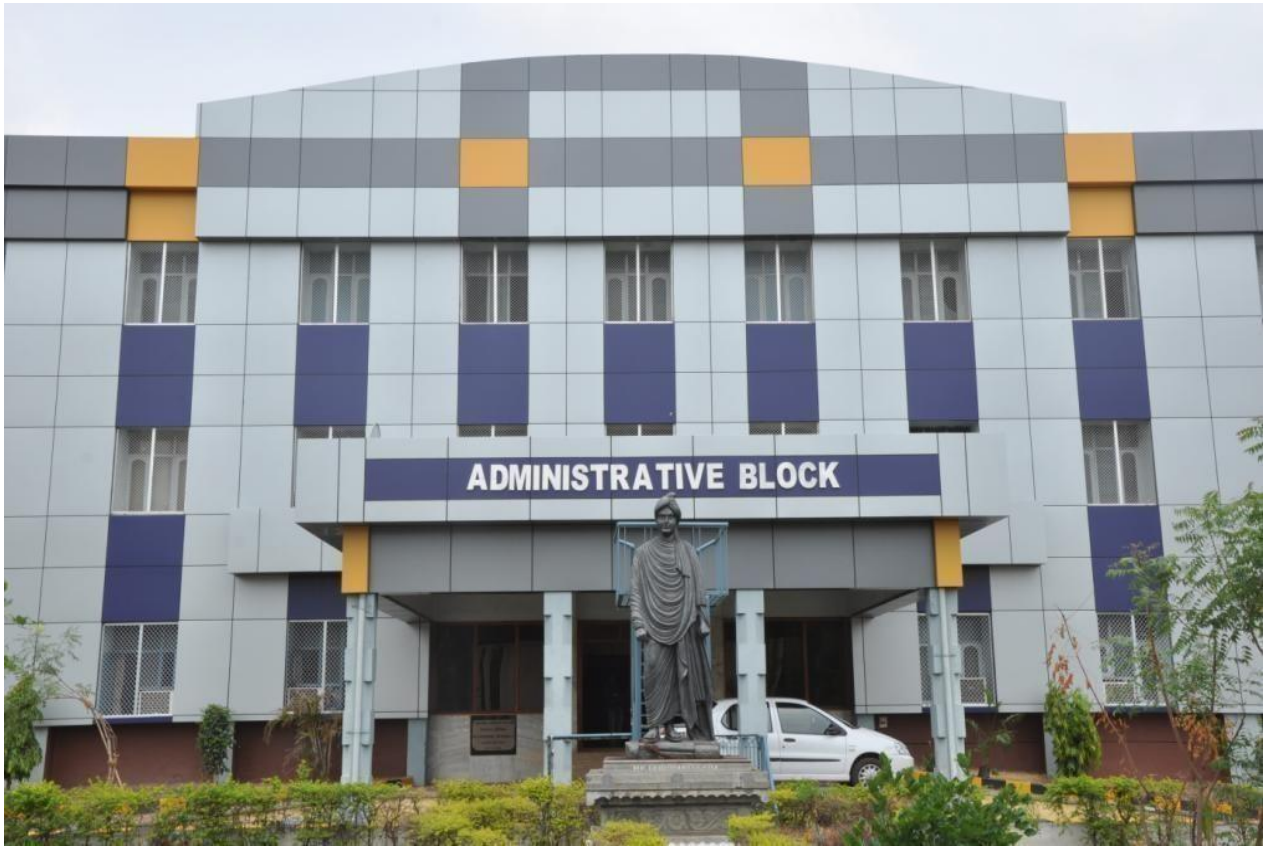
G. PULLA REDDY ENGINEERING COLLEGE (Autonomous):KURNOOL

Accredited by NBA of AICTE and NAAC of UGC with A+ Grade,

Affiliated to JNTUA, Anantapuramu



Scheme – 2020

Scheme and Syllabus for additional courses to be completed for the award of

B.Tech (Honors)

in

Electronics and Communication Engineering

Department of Electronics and Communication Engineering
Honors in Electronics and Communication Engineering
(For ECE students only)

Scheme of instruction and examination

(Effective from 2020-2021)

S No.	Semester	Course Code	Course Title	Credits	Scheme of instruction (periods/ week)		Scheme of Examination Maximum Marks		
					L	T/P	End Exam	Internal Assessment	Total 100
1	IV	HEC01	Detection & Estimation of Signals(DES)	4	4		60	40	100
2	V	HEC02	Application Specific Integrated Circuits (ASIC)	4	3	2	60	40	100
3	VI	HEC03	VLSI Design for Testability (VDFT)	4	4		60	40	100
4	VII	HEC04	Embedded Networks and Protocols (ENP)	4	3	2	60	40	100
5		MOOCS – 1		2	0	0			100
6		MOOCS-2 / Mini Project		2	0	0			100
		Total		**20**					

	MOOCS - 1
1	Microelectronics: Devices to Circuits (Source: IIT Kanpur & NPTEL via SWAYAM)
2	Integrated Photonics Devices and Circuits (Source: IIT Madras & NPTEL via SWAYAM)
3	Mathematical Aspects of Biomedical Electronic System Design (Source: IISc Bangalore & NPTEL via SWAYAM)
4	Signal Processing for mm Wave communication for 5G and beyond (Source: IIT Kharagpur & NPTEL via SWAYAM)
	MOOCS - 2
1	Deep Learning for Computer Vision (Source: NPTEL)
2	Big Data Computing (Source: IIT Patna & NPTEL via SWAYAM)
3	Fabrication Techniques for MEMS-based sensors: clinical perspective (Source: IISc Bangalore & NPTEL via SWAYAM)
4	Introduction to Industry 4.0 and Industrial Internet of Things (Source: IIT Kharagpur & NPTEL via SWAYAM)

DETECTION & ESTIMATION OF SIGNALS (DES)

Scheme: 2020							
Course Code	**Category**	**Hours/Week**		**Credits**	**Maximum Marks**		
HEC01	**PCC**	**L**	**T/P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
		4	**0**	**4**	**40**	**60**	**100**
Sessional Exam Duration: 1½Hrs					**End Exam Duration: 3 Hrs**		

Course Outcomes: At the end of the course the student will be able to

CO1: Understand the basic properties of estimators

CO2: Understand Detection Theory & detection of signals in noise.

CO3: Understand Linear & Nonlinear Estimations.

CO4: Analyze signal detection in noise

CO5: Estimate the parameters of signals in noise

UNIT-I

Introduction: Properties of estimators, Finding good estimators, Estimation of spectrum from finite duration observations.

UNIT-II

Detection Theory: Binary decisions - Single observation. Maximum likelihood decision criterion; Neymann-Pearson criterion; Probability of error criterion; Bayes risk criterion; Minimax criterion; Robust detection; Receiver operating characteristics, Multiple observations.

UNIT-III

Detection of Signals in Noise 1: Minimum probability of Error criterion, Neyman-Pearson criterion for Radar detection of constant and variable, amplitude signals.

UNIT-IV

Detection of Signals in Noise 2: Matched Filters, optimum formulation, detection of random signals, simple problems thereon with multi sample cases.

UNIT-V

Estimation of Signals in Noise: Linear mean squared estimation, non-linear estimates, MAP and ML estimates, maximum likelihood estimate of parameters of linear system, simple problems.

Text Books:

1. Alan V.Oppenheim and Ronald W.Schaffer, *Digital Signal Processing*, PHI,3rd edition,2002
2. J.G.Proakis, *DSP Principles, Algorithms and Applications*, PHI,3rd edition,2002
3. Harry L. Van Trees, "Detection, Estimation and Modulation Theory, Part 1", John Wiley & Sons, edition, 2001.

Reference Books:

1. Steven. M. Kay, *Modern Spectral Estimation, Theory and Applications*, New age International Private Ltd, 2011
2. Shanmugam and Breipohl, *Detection of Signals in Noise and Estimation*, John Wiley & Sons, 2004.
3. Mischa Schwartz, L.Shaw, *Signal Processing: Discrete Sprectral Analysis, Detection, and Estimation, Mc Graw Hill.*

MOOC'S Equivalent Course

https://nptel.ac.in/courses/117/103/117103018/

Question Paper Pattern:

Sessional Exam: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Examination: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions. And the student should answer any one question from each unit. Each Question carries 12 marks.

Internal Assessment: 40M

End Exam: 60M

APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASIC)

Scheme: 2020							
Course Code	**Category**	**Hours/Week**		**Credits**	**Maximum Marks**		
HEC02	**PCC**	**L**	**T/P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
		3	**2**	**4**	**40**	**60**	**100**
Sessional Exam Duration: 1½Hrs				**End Exam Duration: 3 Hrs**			

Course Outcomes: At the end of the course the student will be able to

CO1: Understand the concepts of ASICs

CO2: Understand the design flow of ASICs.

CO3: Understand CMOS system core

CO4: Understand ground rules of MOS circuits

CO5: Understand Logic Synthesis in ASIC design

UNIT-I

Introduction to ASICs: Types of ASICs, Design flow, Economics of ASICs, ASIC Cell Libraries, CMOS Logic, CMOS Design Rules, Logic Cells, I/O Cells, Cell Compilers.

UNIT-II

ASIC Library Design : Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Cell Design, Programmable ASICs, Programmable ASIC Logic Cells, Programmable ASIC I/O Cells, Programmable ASIC Interconnect, Programmable ASIC Design Software

UNIT-III

Design: Low-level Design Entry, Schematic Entry, Low-Level Design Languages, PLA Tools, EDIF, An overview of VHDL and Verilog, Logic Synthesis, Simulation. ASIC Construction, Floor Planning and Placement.

UNIT-IV

CMOS System Core Studies: Dynamic Warp Processors: Introduction, The Problem, The Algorithm, A Functional Overview, Detailed Functional Specification, Structural Floor Plan, Physical Design, Fabrication, Hierarchical Layout And Design Of Single Chip 32 Bit

UNIT-V

Practical Realities and Ground Rules: Further Thoughts on Floor Plans/Layout, Floor Plan Layout of The Four Bit Processors, Input/output (I/O) Pads, "Real estate", Further Thoughts on System Delays, Ground Rules for Successful Design, Scaling of MOS Circuits.

Text Books:

1. Application Specific Integrated Circuits by J.S. Smith, Addison Wesley, 1997.

Reference Books:

1. Basic VLSI Design : Systems and Circuits, Doublas A. Pucknell & Kamran Eshraghian, Prentice Hall of India Private Ltd., New Delhi, 1989.
2. VLSI Design Techniques for analog and digital circuits, R.L. Geiger, P.E. Allen & N.R. Streder, McGraw Hill Int. 1990.

MOOC'S Equivalent Course

https://www.coursera.org/lecture/vlsi-cad-layout/basics-1MtuT

Question Paper Pattern:

Sessional Exam: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Examination: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions. And the student should answer any one question from each unit. Each Question carries 12 marks.

Internal Assessment: 40M

End Exam: 60M

VLSI DESIGN FOR TESTABILITY (VDFT)

Scheme: 2020							
Course Code	**Category**	**Hours/Week**		**Credits**	**Maximum Marks**		
HEC03	**PCC**	**L**	**T/P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
		4	**0**	**4**	**40**	**60**	**100**
Sessional Exam Duration: 1½Hrs				**End Exam Duration: 3 Hrs**			

Course Outcomes: At the end of the course the student will be able to

CO1: Understand all the levels of testing done in VLSI circuits

CO2: Understand the DFT principles in VLSI circuits

CO3: Understand logic and fault simulation in VLSI circuits

CO4: Generate test generation in VLSI circuits

CO5: Understand the BIST technology

UNIT-I

Introduction to Testing: Importance of Testing, Testing During the VLSI Lifecycle, Challenges in VLSI Testing- Challenges in VLSI Testing, Fault Models; Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology

UNIT-II

Design for Testability: Introduction, Testability Analysis----SCOAP Testability Analysis, Probability - Based Testability Analysis, Simulation-Based Testability Analysis; Design for Testability Basics--- Ad Hoc Approach, Structured Approach; Scan Cell Designs--Muxed-D Scan Cell, Clocked-Scan Cell, LSSD Scan Cell; Scan Architectures --- Full-Scan Design, Partial-Scan Design, Random-Access Scan Design; Scan Design Rules, Scan Design Flow diagram and brief description of each stages only, RTL Design for Testability

UNIT-III

Logic and Fault Simulation : Logic Simulation for Design Verification, Fault Simulation for Test and Diagnosis, Simulation Models--- Gate-Level Network, Logic Symbols, Logic Element Evaluation, Timing Models; Logic Simulation, Fault Simulation--- serial, parallel, deductive, concurrent and differential fault simulation; fault detection, comparison of Fault Simulation Techniques, Alternatives to Fault Simulation

UNIT-IV

Test Generation: Introduction, Random Test Generation, Boolean difference, untestable faults, Designing a Stuck-At ATPG for Combinational Circuits--- A Naive ATPG Algorithm, A Basic ATPG Algorithm, D Algorithm, PODEM, PODEM; Designing a Sequential ATPG--- Designing a Sequential ATPG, 5-Valued Algebra Is Insufficient, Gated Clocks and Multiple Clocks; Untestable Fault Identification, ATPG for Non-Stuck-At Faults--- Designing an ATPG That Captures Delay Defects, ATPG for Transition Faults.

UNIT-V

Logic Built-In Self-Test: Introduction, Test Pattern Generation--- Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing; Output Response Analysis--- Ones Count Testing, Transition Count Testing, Signature Analysis, Logic BIST Architectures ---- BIST Architectures for Circuits without Scan Chains, BIST Architectures for Circuits with Scan Chains, BIST Architectures Using Register Reconfiguration, BIST Architectures Using Concurrent Checking Circuits, Fault Coverage Enhancement, BIST Timing Control

Text Books:

1. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, "VLSI Test Principles and Architectures: Design for Testability", 1st Edition, Morgan Kaufmann, 2006.

Reference Books:

1. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers, 2000
2. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House,2002

MOOC'S Equivalent Course

https://onlinecourses.nptel.ac.in/noc20_ee76/preview

Question Paper Pattern:

Sessional Exam: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Examination: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions. And the student should answer any one question from each unit. Each Question carries 12 marks.

Internal Assessment: 40M

End Exam: 60M

EMBEDDED NETWORKS AND PROTOCOLS (ENP)

Scheme: 2020							
Course Code	**Category**	**Hours/Week**		**Credits**	**Maximum Marks**		
HEC04	**PCC**	**L**	**T/P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
		3	**2**	**4**	**40**	**60**	**100**
Sessional Exam Duration: 1½Hrs					**End Exam Duration: 3 Hrs**		

Course Outcomes: At the end of the course the student will be able to

CO1: Understand concepts of CAN protocols and ethernet.

CO2: Understand elements of a network.

CO3: Understand Embedded Ethernet

CO4: Understand industrial networking protocols.

CO5: Understand RF communication

UNIT-I

Introduction To CAN: The CAN bus - General - Concepts of bus access and arbitration - Error processing and management - From concept to reality -Patents, licenses and certification – CAN protocol: 'ISO 11898-1'- Content of the different ISO/OSI layers of the CAN bus-Compatibility of CAN 2.0A and CAN 2.0B

UNIT-II

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT-III

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT-IV

Industrial Networking Protocol: LIN – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus - Audiovideo buses - I2C Bus - D2B (Domestic digital) bus - MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'- profi bus.

UNIT-V

RF Communication: Radio-frequency communication: internal and external - Remote control of opening parts - PKE (passive keyless entry) and passive go- TPMS (tyre pressure monitoring systems) -Wireless networks GSM-Bluetooth - IEEE 802.11x - NFC (near-field communication).

Text Books:

1. Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire, Dominique Paret, John Wiley & Sons Ltd- 2007.
2. Embedded Ethernet and Internet Complete, Jan Axelson Penram publications

Reference Books:

1. Embedded networking with CAN and CAN open. Glaf P.Feiffer, Andrew Ayre and Christian Keyold Embedded System Academy 2005
2. Principles of Embedded Networked Systems Design, Gregory J. Pottie, William J. Kaiser Cambridge University Press, Second Edition, 2005.

MOOC'S Equivalent Course

https://onlinecourses.swayam2.ac.in/cec21_cs19/preview

Question Paper Pattern:

Sessional Exam: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Examination: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions. And the student should answer any one question from each unit. Each Question carries 12 marks.

Internal Assessment: 40M

End Exam: 60M