

G. PULLA REDDY ENGINEERING COLLEGE (Autonomous): KURNOOL
Accredited by NBA of AICTE and NAAC of UGC with A+ Grade,
Affiliated to JNTUA, Anantapuramu



Scheme – 2020

Scheme and Syllabus for additional courses to be completed for the award of

B.Tech (Honors)

in

Electrical & Electronics Engineering

Department of Electrical & Electronics Engineering
Honors in Electrical & Electronics Engineering
 Scheme of instruction and examination
 (Effective from 2020-2021)

Scheme: 2020

S No	SEMESTER	COURSE CODE	COURSE NAME	L-T-P	CR
POOL-1					
1	IV	HEE01	Reactive Power Compensation & Management	3-1-0	4
2		HEE02	Data Communications and Networking	3-1-0	4
3		HEE03	Advanced Power Semiconductor Devices	3-1-0	4
4		HEE04	Programmable Logic Controller and Its Applications	3-1-0	4
POOL-2					
1	V	HEE05	Power System Deregulation	3-1-0	4
2		HEE06	Cellular and Mobile Communications	3-1-0	4
3		HEE07	Advanced Power Electronic Converters	3-1-0	4
4		HEE08	Advance Control Systems	3-1-0	4
POOL-3					
1	VI	HEE09	Advanced Power System Protection	3-1-0	4
2		HEE10	Embedded Systems and Programming	3-1-0	4
3		HEE11	PWM Converters & Applications	3-1-0	4
4		HEE12	Digital Control Systems	3-1-0	4
POOL-4					
1	VII	HEE13	Power System Stability & Control	3-1-0	4
2		HEE14	Introduction to VLSI Design	3-1-0	4
3		HEE15	Modelling & Simulation of Power Converters	3-1-0	4
4		HEE16	SCADA Systems and Sequence of Event Recording System	3-1-0	4
1	MOOC-1				2
2	MOOC-2/Mini Project				2
Total Credits					20

REACTIVE POWER COMPENSATION & MANAGEMENT (RPCM)

B.Tech. EEE (Honors) – POOL-1					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE01	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand objectives specifications of load compensation								
CO2: Understand the types of reactive power compensation								
CO3: Understand the concept of demand side management								
CO4: Understand the concept reactive power compensation equipment								
CO5: Understand the concept of reactive power management in electric traction system.								
UNIT - I								
Load Compensation	Objectives and specifications – Reactive power characteristics – Inductive and capacitive approximate biasing – Load compensator as a voltage regulator – Phase balancing and power factor correction of unsymmetrical loads - Examples.							
UNIT - II								
Steady State & Transient state Reactive Power Compensation in Transmission System	Uncompensated line – Types of compensation – Passive shunt and series and dynamic shunt compensation – Characteristic time periods – Passive shunt compensation – Static compensations - Series capacitor compensation – Compensation using synchronous condensers – Examples.							
UNIT - III								
Reactive Power Coordination & Demand side Management	Objective – Mathematical modeling – Operation planning – Transmission benefits – Basic concepts of quality of power supply – Disturbances - Steady – state variations – Effects of under Voltages – Frequency – Harmonics, radio frequency and electromagnetic interferences. Load patterns – Basic methods load shaping – Power tariffs - KVAR based tariffs penalties for voltage flickers and Harmonic voltage levels							
UNIT - IV								
Distribution & User side Reactive Power Management	System losses – Loss reduction methods – Examples – Reactive power planning – Objectives – Economics Planning capacitor placement – Retrofitting of capacitor banks - KVAR requirements for domestic appliances – Purpose of using capacitors – Selection of capacitors – Deciding factors – Types of available capacitor, characteristics and Limitations.							
UNIT - V								
Reactive Power Management in Electric traction Systems and Arc Furnaces	Typical layout of traction systems – Reactive power control requirements – Distribution transformers - Electric arc furnaces – Basic operations- Furnaces transformer – Filter requirements – Remedial measures – Power factor of an arc furnace.							
Text Books								

1. J.E.Miller, Reactive Power Control in Electric Power Systems, John Wiley and Sons, 1982
2. D.M.Tagare, Reactive power Management, Tata McGraw Hill, 2004.
Reference Books
1. H.M.Alassouli, “Reactive power compensation”, Blurb, Incorporated, 2020.
2. Wolfgang Hofmann, Jurgen Schlabbach, Wolfgang Just “Reactive Power Compensation: A Practical Guide”, Wiely publication, 4th Edition, 2012.
Web References:
1. https://www.iare.ac.in/sites/default/files/IARE_RPCM_LN.pdf
2. https://www.scribd.com/presentation/385273934/17119-Unit-2-Theory-of-Steady-State-Reactive-Power-Compensation-in-Electric-Transmission
3. https://www.researchgate.net/publication/317013549_Demand_response_strategy_management_with_active_and_reactive_power_incentive_in_the_smart_grid_A_two-level_optimization_approach
4. https://ieeexplore.ieee.org/document/7339816
5. https://www.researchgate.net/publication/234778470_Adaptive_control_of_the_active_power_of_an_electric_arc_furnace
Question Paper Pattern:
Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.
End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

DATA COMMUNICATIONS AND NETWORKING (DCN)

B.Tech. EEE (Honors) – POOL-1					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE02	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Acquire the knowledge about the layered structure of reference models for computer networks, the concepts of Physical Layer like transmission media, transmission impairments, data modems, switching and multiplexing standards								
CO2: Understand the principles of Error detection, error correction, Flow control, medium access control in the Data Link Layer and IEEE standards for LANs.								
CO3: Understand the various types of static and dynamic routing algorithms, congestion control and avoidance in Network Layer								
CO4: Analyze the Process to Process Delivery using TCP, UDP in transport layer and the cryptography algorithms like DES and RSA in session layer.								
CO5: Understand various application layer protocols like DNS, FTP, HTTP, WWW, SMTP, SNMP								
UNIT – I								
Introduction to Data Communication Networks	Network Services and Architecture. The Internet, Protocols and Standards, Network Models: Layered Tasks, OSI Reference model, TCP/IP Protocol suite, Data communication circuits, Serial and parallel data transmission, Data communication circuit arrangements.							
Physical Layer and Media	Periodic Analog Signals, Digital Signals, Transmission impairment, Data Rate Limits, Performance., Transmission media, Data modems, Switching and Multiplexing (FDM, TDM & WDM).							
UNIT - II								
Data Link Layer	Introduction, Framing, Error Detection and Correction- Parity, LRC, CRC, Hamming code, Flow and Error Control Protocols, HDLC, Multiple Access: Aloha, Controlled Access, Channelization, IEEE Standards: Standard Ethernet, Changes in the Standard, Fast Ethernet, Gigabit Ethernet, wireless LANs.							
UNIT – III								
Network Layer	Virtual circuit and datagram approach in subnets, Shortest path routing, Flooding, Hierarchical routing, Broadcast routing, multicast routing and distant vector routing algorithms, Congestion control algorithms							
UNIT - IV								
Transport Layer	Transport services, addressing, upward and downward multiplexing, TCP and UDP.							
Session Layer	Encryption, Ciphers, Types of ciphers, DES Algorithm, Public key cryptography- RSA Algorithm.							
UNIT - V								
Application Layer	DNS, DNS in internet, FTP, HTTP, WWW, SMTP, SNMP							
Text Books								
1. Behrouz.A. Forouzan, Data communications and Networking, Second edition, TMH, 2003								
2. Andrew S. Tanenbaum, Computer Networks, Third edition, PHI, 2001								

3. Wayne Tomasi (2005), Introduction to Data Communications and Networking, Pearson Education, India.

Reference Books

1. William Stallings, Data and Computer Communications, 3rd edition, Pearson, 2007.

Web References:

1. <https://nptel.ac.in/courses/106105081/>

2. <https://nptel.ac.in/downloads/106105080/>

3. <https://nptel.ac.in/courses/106106091/>

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

ADVANCED POWER SEMICONDUCTOR DEVICES (APSD)

B.Tech. EEE (Honors) – POOL-1					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE03	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the static and dynamic characteristics of current controlled power semiconductor devices.								
CO2: Understand the static and dynamic characteristics of voltage controlled power semiconductor devices								
CO3: Select the devices for different power electronics applications								
CO4: Understand the control and firing circuit for different devices.								
CO5: Understand protection for semiconductor devices								
UNIT – I								
Introduction	Power switching devices, overview – Attributes of an ideal switch, application requirements, Device selection strategy – On-state and switching losses – Power diodes - Types, forward and reverse characteristics, switching characteristics – rating.							
UNIT - II								
Current Controlled Devices	BJT's – Construction, static characteristics, switching characteristics; Negative temperature co-efficient and secondary breakdown; Power darlington – Thyristors – Physical and electrical principle underlying operating mode, Two transistor analogy – concept of latching; Gate and switching characteristics; converter grade and inverter grade and other types; series and parallel operation.							
UNIT – III								
Voltage Controlled Devices	Power MOSFETs and IGBTs – Principle of voltage controlled devices, construction, types, static and switching characteristics, steady-state and dynamic models of MOSFET and IGBTs - Basics of GTO, MCT (MOS Controlled Thyristor), FCT(Field Controlled Thyristor), RCT(Reverse Conducting Thyristor).							
UNIT - IV								
Firing and Protecting Circuits	Necessity of isolation, pulse transformer, optocoupler – Gate drives circuit: SCR, MOSFET, IGBTs and base driving for power BJT. - Over voltage, over current and gate protections; Design of snubbers.							
UNIT - V								
Thermal Protection	Heat transfer – conduction, convection and radiation; Cooling – liquid cooling, vapour – phase cooling; Guidance for heat sink selection – Thermal resistance and impedance -Electrical analogy of thermal components, heat sink types and design.							
Text Books								
1. Rashid M. H., "Power Electronics Circuits, Devices and Applications", Prentice Hall India, Third Edition, New Delhi.								
2. B.W. Williams 'Power Electronics: Devices, Drivers, Applications and Passive Components, Tata McGraw Hill.								

Reference Books

1. Advanced power electronics converters by Euzeli dos santos, Edison R. da silva.
2. Fundamentals of Power Semiconductor Devices by B. Jayanth Baliga, Springer Press, 2008.

Web References:

1. <https://nptel.ac.in/courses/108/107/108107128/>
2. <https://nptel.ac.in/courses/108/108/108108122/>
3. <https://nptel.ac.in/courses/108/102/108102145/>

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

PROGRAMMABLE LOGIC CONTROLLER AND ITS APPLICATIONS (PLC)

B.Tech. EEE (Honors) – POOL-1					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE04	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: The purpose of this course is to understand the Fundamental concept of Automation.								
CO2: To Understand the history of automation from 1st generation (relay based) to the latest and most modern technology used in automation								
CO3: To understand the methods of integrating various components of automation like PLC, sensors, transducers, AC drives, hydraulics and pneumatics learnt in the previous semester.								
UNIT – I								
Introduction to Automation	Introduction to 1st generation automation, advent of microcontroller and the introduction of logic controller. Difficulties of logic controller and the advent of programmable logic controllers. Classification of PLC based on the I/O, parts of plc, like CPU, Chassis, Power supply, I/O module etc.							
UNIT - II								
Input and output system, CPU system	List of input and output device, methods of connecting input devices like source and sink. Methods of connecting output devices. CPU SCAN diagram, introduction to analog input and output, special inputs like high speed inputs etc. introduction of interface of encoders, lvdt, ultrasonic sensor, optical sensor, AC drives, stepper motors, switches and lamps (sensors covered in previous semester).							
UNIT – III								
PLC Programming	Different methods of programming the PLC. Introduction to ladder programming, Data structures like I, Q, AI, AQ, M, R etc., instructions like NO,NC, Transition coils, set/reset coils, timers, counters, control functions, relational functions, arithmetic functions.							
UNIT - IV								
Pneumatic systems	Programming examples, for applications like cranes, ice vending machines, conveyors, Traffic lights, pick and place mechanism using sensors and VFDs.							
UNIT - V								
HMI – Human machine interface systems	Introduction to HMI and need for using HMI. Different features of HMI and its methods of configuration. Use of HMI to above mentioned applications.							
Text Books								
1. F.G Shinsky., Process control systems: Application, Design and Tuning, 4/e, McGrawHill, 1996								
2. P.R Be.langer, Control Engineering: A Modern Approach, Saunders College Publishing, 1995.								
3. R.C .Dorf and Bishop R. T. , Modern Control Systems, 11/e, Addison Wesley Longman., 2008								
Reference Books								
1. P.A Laplante., Real Time Systems: An Engineer.s Handbook, PHI, 2007.								
2. CH. Houpis and Gary B. Lamont, Digital Control systems, McGraw Hill, 1985.								
3. Programmable Logic Controllers: Principles and Applications, Webb &Reis, PHI								

Web References:

1. <https://www.electrical4u.com/programmable-logic-controllers/>
2. <https://www.watelectrical.com/industrial-applications-of-programmable-logic-controller/>
3. <https://nptel.ac.in/content/storage2/courses/112103174/>

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

POWER SYSTEM DEREGULATION (PSD)

B.Tech. EEE (Honors) – POOL-2					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE05	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the process and operation of restructured powersystem.								
CO2: Understand knowledge on fundamental concepts of congestion management.								
CO3: Analyze the concepts of locational marginal pricing and financial transmission Rights.								
CO4: Understand the concept of Ancillary Service management.								
CO5: Understand knowledge on Reforms in Indian Power Sector.								
UNIT – I								
Introduction to Restructuring of Power industry	Introduction: Deregulation of power industry, Restructuring process, Issues involved in deregulation, Deregulation of various power systems – Market models: Comparison of various market models, OASIS: Open Access Same–time Information System – structure of oasis – pooling of information – transfer capability on OASIS.							
UNIT - II								
Transmission Congestion Management	Introduction: Definition of Congestion, reasons for transfer capability limitation, Importance of congestion management, Features of congestion management – Classification of congestion management methods. Definitions transfer capability issues: – ATC – TTC – TRM – CBM calculations –methodologies to calculate ATC.							
UNIT – III								
Locational Marginal prices and Financial transmission rights	Mathematical preliminaries: -Locational marginal pricing– Lossless DCOPF model for LMP calculation – Loss compensated DCOPF model for LMP calculation – ACOPF model for LMP calculation – Financial Transmission rights.							
UNIT - IV								
Ancillary Service management and pricing of Transmission rights	Introduction of ancillary services – Types of Ancillary services – Classification of Ancillary services – Load generation balancing related services – Voltage control and reactive power support devices – Black start capability service - ancillary service –Co- optimization of energy and reserve services - International comparison - Transmission pricing – Principles – Classification – Role in transmission pricing methods – Marginal transmission pricing paradigm –							
UNIT - V								
Reforms in Indian Power Sector	Introduction – Framework of Indian power sector – Reform initiatives - Availability based tariff – Electricity act 2003 – Open access issues – Power exchange – Reforms in the near future.							
Text Books								
1. Mohammad Shahidehpour, Muwaffaq Alomoush, Marcel Dekker, “Restructured electrical power								

systems: operation, trading and volatility” Pub., 2001.
2. Kankar Bhattacharya, Jaap E. Daadler, Math H.J. Boolen, “Operation of restructured power systems”, Kluwer Academic Pub., 2001.
3. Kimbark E.W. “Power system stability and control – Vol III, synchronous machines”, John Wiley & Sons.
Reference Books
1. Ajay Pandey Sebastian Morris, Electricity Reforms and Regulations -A Critical Review of Last 10 Years Experience, Indian Institute of Management Ahmedabad, 2009.
2. Loi Lei Lai, 'power system restructuring and Deregulation' , John Wiley & Sons Ltd., England.
3. Sally Hunt, “Making competition work in electricity”, John Willey and Sons Inc. 2002.
4. Steven Stoft, “Power system economics: designing markets for electricity”, John Wiley & Sons, 2002.
Web References:
1. https://nptel.ac.in/courses/108/101/108101005/
2. https://www.researchgate.net/publication/241181846_Transmission_Congestion_Management_in_restructured_power_systems
3. https://ieeexplore.ieee.org/abstract/document/8326042
4. https://eal.iitk.ac.in/assets/docs/Rohit_Bajaj_Ancillary.pdf
5. https://home.kpmg/xx/en/home/industries/government-public-sector/international-development-services/strategy-and-policy-implementation/structural-reforms-in-the-indian-power-sector.html
Question Paper Pattern:
Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.
End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

CELLULAR AND MOBILE COMMUNICATIONS (CMC)

B.Tech. EEE (Honors) – POOL-2					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE06	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	2	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the fundamental concepts of cellular & mobile communication and its Radiopropagation.								
CO2: Understand the cell site and mobile antennas								
CO3: Analyze various types of handoffs and analog and digital switching equipment								
CO4: Analyze different ARQ techniques and multiple access schemes								
CO5: Understand the GSM architecture, SS7 protocol model, AIN for mobile communication								
UNIT - I								
Introduction	Basic Cellular System, Operation of Cellular system, Hexagonal cells, Frequency reuse of channels, Co-channel interference reduction, Cell splitting.							
Cell Coverage for signal and traffic	Incident, Reflection & Elevation angles, Point to point model, Path loss formula, propagation over water or flat Open Area, Land-to mobile transmission, path loss from point to point prediction model, Mobile to Mobile propagation.							
UNIT - II								
Cell site Antennas & Mobile Antennas	Antenna at cell site and mobile antennas							
Frequency Management & Channel Assignment	Frequency management, Frequency-spectrum utilization, Set-up channels, Channel assignment to cell site & mobile units, Fixed & non-fixed channel assignment							
UNIT - III								
Hand offs	Why hand off (H.O), Types of H.O, Initiation of H.O, Delaying H.O, Forced H.O, Queuing H.O, Power difference H.O, Mobile assisted H.O, Soft H.O, Intersystem H.O.							
Switching & Traffic	Space & Time switching, Analog switching equipment for cellular mobile system, Cellular digital switching equipment, MTSO inter connections.							
UNIT - IV								
Introduction to Digital Mobile Telephony	Introduction to digital technology, ARQ techniques, Stop and wait ARQ, Selective reference mission with ARQ, Multiple access schemes.							
UNIT - V								
Digital Cellular System	Global system for mobile communication (GSM), GSM architecture, layer modeling, Transmission, GSM channels & channel modes, Radio resources management, Mobility management, Communication management, Network management.							
Intelligent Network for	Advanced intelligent network (AIN) & Its architecture, SS7 protocol model, AIN for mobile communication							

Wireless Communication	
Text Books	
1. Lee William.C.Y, Mobile Cellular Telecommunications Analog and Digital System, Mc Graw Hill, 2nd Edition.	
2. T.S.Rappaport, Wireless communications, Pearson Ed, 2nd Edition.	
Reference Books	
1. Pandya Raj, Mobile and Personal Communication Services and Systems, PHI, 2nd Edition, March, 2004.	
2. Jochen Schiller H, Mobile Communications, Pearson Ed, 2nd Edition, 2008.	
Question Paper Pattern:	
Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.	
End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.	

ADVANCED POWER ELECTRONIC CONVERTERS (APEC)

B.Tech. EEE (Honors) – POOL-2					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE07	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Get Knowledge on Isolated and Non isolated DC-DC converters								
CO2: Get Knowledge on resonant DC-DC converters								
CO3: Get Knowledge DC-AC converters								
CO4: Get Knowledge on PWM techniques								
CO5: Get Knowledge on AC-DC Converters.								
UNIT - I								
DC-DC Converters	Introduction, Simple DC to DC converters, Non-Isolated DC-DC converters- Buck, Boost, Buck-Boost; Isolate DC-DC Converters – Forward Converter, Push-Pull Converter, Half and Full Bridge converters and Fly back converter.							
UNIT - II								
RESONANT CONVERTERS	Resonant converters – zero current switching resonant converters – L type ZCS resonant converter – M type ZCS resonant converter – zero voltage switching resonant converters – comparison between ZCS and ZVS resonant converters – Two quadrant ZVS resonant converters – resonant dc-link inverters – evaluation of L and C for a zero current switching inverter.							
UNIT - III								
DC-AC Converters	Introduction to Inverters, Multilevel concept – Classification of multilevel inverters – Diode clamped Multilevel inverter, improved diode Clamped inverter, Flying capacitors multilevel inverter, cascaded multilevel inverter – principle of operation – main features.							
UNIT - IV								
PWM techniques for power converters	Pulse width modulation techniques for bridge converters, Bus clamping PWM, Space vector based PWM, Advanced PWM techniques.							
UNIT - V								
AC to DC converters	Single Phase Converter, Three Phase Converter, Effect of Source Inductance and PWM Rectifiers PWM Rectifiers and Power Factor Improvement Techniques.							
Text Books								
1. Mohammed H. Rashid, “Power Electronics”– Pearson Education-Third Edition – first Indian reprint - 2004.								
2. B.K Bose, “ Modern Power Electronics and AC drives -Hall of India Pvt. Ltd., New Delhi								
3. V. Ramanarayanan, “Course Material on Switched Mode Power Conversion” Narosa Publications								
Reference Books								
1. L. Umanand, “ Power Electronics: Essentials & Applications” Wiley Publishers								
Web References:								
1. https://nptel.ac.in/courses/108/107/108107128/								
2. https://nptel.ac.in/courses/108/102/108102145/								

3. <https://nptel.ac.in/courses/108/108/108108035/>

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

ADVANCE CONTROL SYSTEMS (ACS)

B.Tech. EEE (Honors) – POOL-2					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE08	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Analyze dynamics of a linear system by solving system model/equation or applying domain transformation.								
CO2: Realize the structure of a discrete time system and model its action mathematically.								
CO3: Examine a system for its stability, controllability and observability.								
CO4: Implement basic principles and techniques in designing linear control systems.								
CO5: Formulate and solve deterministic optimal control problems in terms of performance indices.								
UNIT – I								
Introduction	Introduction to control systems - properties of signals and systems - convolution integral - ordinary differential equation - Transfer function - Pole zero concepts - effect of pole location on performance specification - System models in state space, canonical model, MIMO systems - Solution of state equation - stability of systems in state space.							
UNIT - II								
Linear System Transformation	Linear algebra, vector spaces, span and change of basis - linear transformations - Gram Schmidt orthogonalization criterion - QR decomposition – Singular value decomposition.							
UNIT – III								
Linear System Analysis	Computing eAT controllability - Observability controller design, observer design, reduced order observers, properties of controllability - Computing numerical rank of a matrix - Kalman canonical forms, partial pole assignment using static pole output feedback - Design of non-interacting systems.							
UNIT - IV								
Non-linear system analysis	Non-linear system behavior - different methods of linearization - Lyapunov stability criterion – Phase plane analysis, singular points, constructing phase portraits, existence of limit cycle.							
UNIT - V								
Describing function analysis	Fundamentals, assumptions, definitions - Describing functions of common non-linearity's -Describing function analysis of non-linear system - Stability of limit cycles, reliability of describing function analysis.							
Text Books								
1. Robert E. Skelton, “Dynamic System Control and Linear System Analysis and Synthesis”, John Wiley and Sons Inc., New Delhi, 1988.								
2. B. C. Kuo, “Automatic Control Systems”, PHI Learning, 7 th edition, 1995								
3. M.Gopal, “Modern Control Systems”, New Age International, 2 nd edition, 1993								
4. Brogan W. L., “Modern Control Theory”, Prentice Hall International, New Jersey, 1991.								
Reference Books								
1. Jean Jacques E. Slotine, Weiping Autor Li, “Applied Nonlinear Control”, Prentice Hall Inc., 1991.								

2. M. Vidyasagar, "Nonlinear System Analysis", Prentice Hall Inc., 2nd Edition, 1993.

Web References:

1. portal.tpu.ru:7777/SHARED/s/SMIKE/Uchebnaya/.../Modern_Control_Engineering.pdf

2. [www.znu.ac.ir/data/members/pirmohamadi_ali/Control/Brogan\(BookZZ.org\).pdf](http://www.znu.ac.ir/data/members/pirmohamadi_ali/Control/Brogan(BookZZ.org).pdf)

3. sv.20file.org/up1/951_0.pdf

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

ADVANCED POWER SYSTEM PROTECTION (APP)

B.Tech. EEE (Honors) – POOL-3					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE09	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the knowledge on zones of protection in static relays.								
CO2: Understand the concept on comparators used in static relays.								
CO3: Understand the concept over current, differential and distance relays.								
CO4: Understand the stability analysis and time domain analysis								
CO5: Understand the concept of Microprocessor Based Protective relays.								
UNIT – I								
Introduction	Need for protection systems: Nature and causes of faults, types of faults, effects of faults, fault statistics, evolution of protective relays, zones of protection, primary & back up protection, essential qualities of protection.							
Static Relays	Advantages of static relays-Basic construction of static relays-Level detectors-Replica impedance –Mixing circuits-General equation for two input phase and amplitude comparators-Duality between amplitude and phase comparators							
UNIT - II								
Amplitude Comparators	Circulating current type and opposed voltage type- rectifier bridge comparators, Direct and Instantaneous comparators.							
Phase Comparators	Coincidence circuit type- block spike phase comparator, techniques to measure the period of coincidence-Integrating type-Rectifier and Vector product type-Phase comparators							
UNIT – III								
Static Over Current Relays	Instantaneous over-current relay-Time over-current relays-basic principles –definite time and Inverse definite time over-current relays.							
Differential Relays	Analysis of Static Differential Relays –Static Relay schemes –Duo bias transformer differential protection –Harmonic restraint relay.							
Static Distance Relays	Static impedance-reactance–MHO and angle impedance relay-sampling comparator –realization of reactance and MHO relay using sampling comparator.							
UNIT - IV								
Carrier-Aided Protection of Transmission Lines	Need for Carrier-aided Protection, Coupling and Trapping the carrier into the Desired Line Section.Unit Type Carrier-aided Directional Comparison Relaying, Carrier-aided Distance Schemes for Acceleration of ZoneII, Phase Comparison Relaying(Unit Scheme)							
Induction Motor Protection	Introduction, Various Faults and abnormal operating Conditions, Starting Current, Electrical faults, Abnormal Operating Conditions from supply side, Operating Conditions from Mechanical side,Data required for Designing Motor protection Schemes.							
UNIT - V								

Numerical Protection	Introduction,Block diagram of numerical Relay, Sampling theorem, Correlation with a Reference wave, Fourier Analysis of Analogue Signal,Least Error Squared(LES) Technique, Digital Filtering, Numerical Over-current Protection, Numerical Transformer Differential protection, Numerical Distance Protection of Transmission Line, Mann and Morrison Method, Differential Equation method.
Text Books	
1. Badri Ram and D.N.Vishwakarma, “Power system protection and Switch gear”, TMH publication New Delhi 1995.	
2. T.S. MadhavaRao, Power system protection Static relays, TMH 2nd edition 1981	
3. Y.G.Paithankar,S.R.Bhide, “Fundamentals of Power System Protection” PHI publications.	
Reference Books	
1. Mason, The Art and Science of protective relaying, Wiley Eastern Ltd.	
2. C.L. Wadhwa, Electrical power systems, New age International (P) Limited.	
3. Sunil S. Rao, Switchgear and protection, Khanna Publications	
Web References:	
1. https://www.slideshare.net/jawaharramaya/static-relay	
2. https://www.engineeringenotes.com/electrical-engineering/comparators/phase-comparators-and-its-types-devices-electrical-engineering/32832	
3. https://www.electrical4u.com/differential-relay/#:~:text=The%20differential%20relay%20is%20one,of%20an%20electrical%20power%20circuit.	
4. https://www.elprocus.com/induction-motor-protection-system-circuit-working/#:~:text=Induction%20motor%20Protection%20system%20from,system%20is%20violating%20its%20rating.	
5. https://en.wikipedia.org/wiki/Numerical_relay .	
Question Paper Pattern:	
<p>Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.</p> <p>End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.</p>	

EMBEDDED SYSTEMS AND PROGRAMMING (ESP)

B.Tech. EEE (Honors) – POOL-3					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE10	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the characteristics, attributes and applications of Embedded Systems								
CO2: Understand the core structure and microcontroller ports for Embedded applications								
CO3: Analyze the functions and data types of Embedded C in interfacing ports of microcontrollers								
CO4: Utilize the architecture and programming model of MSP 430 for peripheral interface								
CO5: Understand the architecture and programming model of ARM processors.								
UNIT – I								
INTRODUCION	Definition of Embedded System, Embedded Systems Vs General Computing Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.							
UNIT - II								
CORE EMBEDDED SYSTEMS	OF	Programming languages for embedded systems, Structural units in embedded processor, Microcontroller Port Structures, Timer Concepts, Interrupts.						
UNIT – III								
PROGRAMMING IN C	Introduction to Embedded C, Data types Functions Hello world program Super Loop architecture, delay function, Controlling the port pins, Reading switches, Basic techniques for reading and writing the port pins, Example: Counting goats.							
UNIT - IV								
MSP430	Family, Architecture – MSP430, Address Space, On Chip Peripherals and Register sets, Addressing Modes, Programming GPIO Interfaces in C language- LED, Switches, Motor.							
UNIT - V								
ARM Processor	ARM Design Philosophy, RISC vs CISC, ARM 7 and 9 processor family, Block Diagram, Registers, Program Status Register, Five Stage Instruction Pipeline, and Architecture Revision. Instruction Set: Data Processing Instructions, Addressing Mode. Introduction to Thumb Instruction Set.							
Text Books								
1. Frank Vahid, Embedded System Design, 2nd Edition Wiley Publications, 2009								
2. Michael J. Point, Embedded C, 1st Edition, A Pearson Education, 2002								
3. John H. Davies, MSP430 Microcontroller Basics, Elsevier, 2008								
4. Steve Furber, ARM System on Chip Architecture, 2nd Edition, Addison Wesley Professional, 2000								
Reference Books								
1. Raj Kamal, Embedded Systems Architecture, Programming and design, 2nd Edition, TMH, 2006								
2. Arnold S Burger, Embedded System Design An Introduction to Processes, Tools and Techniques, 1st Edition, CMP Books, 2007								
3. Shibu K.V, Introduction to Embedded Systems, Tata Mc Graw Hill, 2009								

Web References:

1. www.nptel.onlinecourse.ac.in/embeddedsystemsdesgin.
2. www.nptel.onlinecourse.ac.in/microcontrollersapplications.

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

PWM CONVERTERS AND APPLICATIONS (PWMCP)

B.Tech. EEE (Honors) – POOL-3					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE11	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Knowledge concepts and basic operation of PWM converters, including basic circuit operation and design								
CO2: Learn the steady-state and dynamic analysis of PWM converters along with the applications like solid state drives and power quality								
CO3: Able to recognize and use the following concepts and ideas: Steady-State and transient modeling and analysis of power converters with various PWM techniques								
UNIT – I								
PWM Techniques for Two-level inverter	Carrier-Based Pulse Width Modulation for Two-level Three-phase Voltage Inverters, Space Vector Modulation Strategies, Overmodulation of Three-phase Voltage source inverters.							
UNIT - II								
PWM Techniques for Multi-level inverter	Carrier-Based Pulse Width Modulation, Space Vector Modulation Strategies, Overmodulation for Three-phase Multilevel Voltage source Inverters.							
UNIT – III								
Applications of power converters	Compensation for dead time and DC voltage regulation, Dynamic model of PWM converter. Multilevel converters, Constant V/f induction motor drives.							
UNIT - IV								
Performance parameters analysis	Estimation of current ripple and torque ripple in inverter fed drives, Line-side converters with power factor compensation. Active power filtering, Reactive power compensation, Harmonic current compensation, Selective harmonic elimination PWM technique for high power electric drives.							
UNIT - V								
Special Drives	PWM converter applications to special Electrical Machines – BLDC motor and switched Reluctance Motor.							
Text Books								
1. Mohan, Undeland and Robbins, “Power Electronics: Converters, Applications and Design”, John’s Wiley and Sons.								
2. Erickson RW, “Fundamentals of Power Electronics”, Chapman and Hall.								
3. Eric Monmasson, “Power Electronic Converters PWM Strategies and Current Control Techniques”, Wiley Publisher.								
Reference Books								
1. Vithyathil. J, “Power Electronics: Principles and Applications”, McGraw Hill.								
2. Rashid M. H., "Power Electronics Circuits, Devices and Applications", Prentice Hall India, Third Edition, New Delhi.								
3. B.K Bose, “Modern Power Electronics and AC drives -Hall of India Pvt. Ltd., New Delhi								

Web References:

1. <https://nptel.ac.in/courses/108/108/108108035/>
2. https://www.youtube.com/watch?v=7vyQZ_mDH5w
3. <https://www.youtube.com/watch?v=xcxFDlz1bEs>

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

DIGITAL CONTROL SYSTEMS (DCS)

B.Tech. EEE (Honors) – POOL-3					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE12	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the basic A/D and D/A conversion								
CO2: Understand the Z- Transform								
CO3: Understand the state space analysis methods								
CO4: Understand the stability analysis and time domain analysis								
CO5: Understand digital process control and design.								
UNIT - I								
Introduction	Block diagram of typical digital control system - advantages of sampling in control systems – examples of discrete data and digital control systems - reconstruction of sampled signals, ZOH.							
Z- Transforms	Definition and evaluation of Z-transforms, mapping between s-plane and z-plane - inverse Z-transform, theorems of Z-transforms - limitation of Z-transform - pulse transfer function - pulse transfer function of ZOH - relation between G(s) and G(z) - signal flow graph method applied to digital systems.							
UNIT - II								
State Space Analysis	State space modeling of digital systems with sample and hold - state transition equation of digital time in variant systems - solution of time in variant discrete state equation by the Z-transformation - transfer function from the state model, Eigen values, Eigen vectors and diagonalisation of the A-matrix, Jordan canonical form, computation of state transition matrix.							
UNIT - III								
Stability	Definition of stability, stability tests, the second method of Lyapunov.							
Time Domain Analysis	Comparison of time responses of continuous data and digital control systems - correlation between time response and root locus in the s-plane and z-plane - root loci for digital control systems - steady state error analysis of digital control systems.							
UNIT - IV								
Controllability and Observability	Theorems on controllability - theorems on observability (time invariant systems) - relation between controllability - observability and transfer function - controllability and observability vs. Sampling period.							
UNIT - V								
Compensation (With Design)	Realization and Design of basic lead, Lag and lead-Lag compensators.							
PID Controllers (With Design)	Digital PID controller - pole placement through state feedback.							
Text Books								
1. B. C. Kuo, “Digital Control Systems”, Oxford University Press, USA, 2nd edition, 1995								

2. M.Gopal, "Digital Control Systems", Wiley; 1st edition, 1988

3. K. Ogata, "Modern Control Engineering", Prentice Hall, 5th edition, 2010

Reference Books

1. Ioan Doré Landau, Gianluca Zito, "Digital Control Systems: Design, Identification and Implementation", Springer Science & Business Media

Web References:

1. <https://link.springer.com/book/10.1007%2F978-1-84628-056-6>

2. <http://www.sciencedirect.com/science/book/9780123943910>

3. <https://nptel.ac.in/courses/108/108/108108035/>

4. <http://www.springer.com/in/book/9781846280559>

5. <http://www.springer.com/in/book/9783642864193>

6. <http://nptel.ac.in/courses/108103008/>

7. <https://www.coursehero.com/file/13785953/DIGITAL-CONTROL-SYSTEMSpdf/>

8. http://een.iust.ac.ir/profs/Esmailzadeh/MSc.%20Digital%20Control%20Systems/Digital%20Control%20System_PhilipsNagle.pdf

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

POWER SYSTEM STABILITY & CONTROL (PSC)

B.Tech. EEE (Honors) – POOL-4					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE13	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand how to develop linear and nonlinear models of multi-machine power systems								
CO2: Understand the concept of Dynamic Stability								
CO3: Analyze various types of stability properties of power systems.								
CO4: Understand how to model and simulate excitation mechanisms in synchronous machines.								
CO5: Analyze controllers for transient/angle stabilization and voltage regulation.								
UNIT – I								
The Elementary Mathematical Model and System Response to Small Disturbances	A Classical model of one machine connected to an infinite bus – Classical model of multimachine system – Problems – Effect of the excitation system on Transient stability. The unregulated synchronous Machine – Effect of small changes of speed – Modes of oscillation of an unregulated multimachine system – Regulated synchronous machine – Voltage regulator with one time lag – Governor with one time lag – Problems.							
UNIT - II								
Dynamic Stability	Concept of Dynamic stability – State space model of one machine system connected to infinite bus – Effect of excitation on Dynamic stability – Examination of dynamic stability by Routh’s criterion.							
UNIT – III								
Power System Stabilizers	Introduction to supplementary stabilizing signals - Block diagram of the linear system - Approximate model of the complete exciter – Generator system – Lead compensation – Stability analysis using eigen value approach							
UNIT - IV								
Excitation Systems	Excitation system response – Non-continuously regulated systems – Continuously regulated systems – Excitation system compensation – State space description of the excitation system - Simplified linear model – Effect of excitation on generator power limits. Type –2 system: Rotating rectifier system, Type-3 system: Static with terminal potential and current supplies - Type –4 system: Non – continuous acting - Block diagram representation – State space modeling equations of these types.							
UNIT - V								
Stability Analysis	Review of Lyapunov’s stability theorems of non-linear systems using energy concept – Method based on first concept – Method based on first integrals – Quadratic forms – Variable gradient method – Zubov’s method – Popov’s method, Lyapunov function for single machine connected to infinite bus. What is voltage stability – Factors affecting voltage instability and collapse – Comparison of Angle and voltage stability – Analysis of voltage instability and collapse – Integrated analysis of voltage and Angle stability – Control of voltage instability							
Text Books								

1. P.M.Anderson, A.A.Fouad, “Power System Control and Stability”, IOWA State University Press, Galgotia Publications, Vol-I, 1 st Edition.
2. PrabhaKundur., “ Power system stability and control”, Tata McGraw Hill.
3. Kimbark E.W. “ Power system stability and control – Vol III, synchronous machines”, John Wiley & Sons.
Reference Books
1. M.A.Pai, Power System Stability-Analysis by the direct method of Lyapunov, North Holland Publishing Company, New York, 1981.
2. K.R. Padiyar, “ Power systems Dynamics stability and control”, Interline publishing Pvt.,ltd., Bangalore.
Web References:
1. https://www.ijareeie.com/upload/2016/june/149_Study.pdf
2. https://nptel.ac.in/content/storage2/courses/108106026/chapter1.pdf
3. https://www.geenergyconsulting.com/practice-area/global-power-projects/power-system-stabilizers#:~:text=Power%20system%20stabilizer%20(PSS)%20control,about%202%20%2D3%20Hz).
4. https://circuitglobe.com/excitation-system.html
5. https://nptel.ac.in/content/storage2/courses/108104051/chapter_9/9_1.html
Question Paper Pattern:
Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.
End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

INTRODUCTION TO VLSI DESIGN (IVLSID)

B.Tech. EEE (Honors) – POOL-4					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE14	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	1	0	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Absorb the ASIC classification and detailed steps followed in modern IC fabrication.								
CO2: Derive the MOSFET I-V characteristics from basic understanding of n, p channel devices.								
CO3: Analyze the CMOS circuits, their characteristics delays, power and transistor sizing.								
CO4: Comprehend other logic variations viz. pass-transistor, dynamic, pseudo NMOS, logic.								
CO5: Grasp the semiconductor memories namely RAMs, ROMs, for their feature set.								
UNIT – I								
VLSI Fabrication Technology	Introduction to ASICs, ASICs classification, Typical ASIC/VLSI Design Flow, IC Fabrication Steps, Art of miniaturization, VLSI Processes: Twin-Well CMOS Process, MOSFET, Resistors, Capacitors, pn junction Diodes, BiCMOS Process, Lateral pnp Transistor, p-Base and Pinched-Base Resistors, VLSI Design Rules, VLSI Layout, Layouts for CMOS Inverter, CMOS NAND and NOR gates, Beyond 20nm Technology- FinFET							
UNIT - II								
Introduction to MOSFETs	Introduction, Device Structure and Physical Operation, Current–Voltage Characteristics, MOSFET Circuits at DC, The Body Effect and Other Topics, Comparison of MOSFET and BJT, Summary, Problems.							
UNIT – III								
CMOS Digital Logic Circuits	Introduction, CMOS Logic-Gate Circuits, Digital Logic Inverters, The CMOS Inverter, Dynamic Operation of the CMOS Inverter, Transistor Sizing, Power Dissipation, Summary, Problems.							
UNIT - IV								
Advanced Topics in Digital IC Design	Introduction, Implications of Technology Scaling in Deep Submicron Designs, Digital IC Technologies, Logic-Circuit Families, Design Methodologies, Pseudo-NMOS Logic Circuits, Pass-Transistor Logic Circuits, Dynamic MOS Logic Circuits, Bipolar and BiCMOS Logic Circuits, Summary, Problems.							
UNIT - V								
Memory Circuits	Introduction, Latches and Flip-Flops, Semiconductor Memories-Types and Architectures, Random- Access Memory (RAM) Cells, Sense Amplifiers and Address Decoders, Read-Only Memory (ROM), CMOS Image Sensors, Summary, Problems.							
Text Books								
1. Adel S. Sedra and Kenneth C. Smith. 2015. Microelectronic Circuits Revised Edition (7thed.). Oxford University Press, Inc., New York, NY, USA.								
2. Neil Weste and David Harris. 2010. CMOS VLSI Design: A Circuits and Systems Perspective (4thed.). Addison-Wesley Publishing Company, USA.								
Reference Books								

1. Jan M. Rabaey, AnanthaChandrakasan, and Borivoje Nikolic. 2008. Digital IntegratedCircuits (3rded.). Prentice Hall Press, Upper Saddle River, NJ, USA .
2. Michael John Sebastian Smith. 2008. Application-Specific Integrated Circuits (1st ed.). Addison-Wesley Professional.
3. Wayne Wolf. 2008. Modern VLSI Design: Ip-Based Design (4th ed.). Prentice Hall PTR, Upper Saddle River, NJ, USA.
4. Douglas A. Pucknell and Kamran Eshraghian. 1994. Basic VLSI Design (3rd Ed.). Prentice-Hall, Inc., Upper Saddle River, NJ, USA.

Web References:

1. <https://nptel.ac.in/courses/117101058/>
2. <https://www.intel.in/content/www/in/en/company-overview/intel-museum.html>
3. <http://global.oup.com/us/companion.websites/9780199339136/>
4. www.cmosvlsi.com/

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

MODELING & SIMULATION OF POWER CONVERTERS (MSPC)

B.Tech. EEE (Honors) – POOL-4					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE15	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	2	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: Understand the basic operation of PWM techniques for inverters and its simulation.								
CO2: Understand Advanced three phase PWM techniques for inverters and its simulation								
CO3: Model three phase multilevel inverters test through simulation								
CO4: Model DC-DC Converters and verify through simulation								
CO5: Develop PV fed converters and verify its performance through simulation								
UNIT – I								
AC-AC Converters	1-phase and 3-Phase AC voltage controller. 1-phase step and step down Cyclo-converters- simulation in Matlab/Simulink							
UNIT - II								
DC-DC Converters	Design and analysis of Buck converter, Boost converter and Buck-boost converter- simulation in Matlab/Simulink. Simple Basic Two stage converters- simulation in Matlab/Simulink							
UNIT – III								
DC-AC converters	1-phase and 3-phase Inverters. PWM techniques- Carrier Comparison Approach – single pulse width modulation method – multiple pulse width modulation - sine PWM method-simulation in Matlab/Simulink.							
UNIT - IV								
High power DC-AC converters	PWM techniques for MLIs – neutral point clamped MLI – cascaded H-bridge MLI – Dual Inverter fed open end winding arrangement- simulation in Matlab/Simulink							
UNIT - V								
PV fed Converters	Modeling of PV system, PV fed DC-AC converters, PV fed DC-DC converters - simulation in Matlab/Simulink.							
Text Books								
1. Mohammed H. Rashid, “Power Electronics”– Pearson Education-Third Edition – first Indian reprint - 2004.								
2. Mohan, Undeland and Robbins, “Power Electronics: Converters, Applications and Design”, John’s Wiley and Sons								
3. Agam Kumar Tyagi, “Matlab and Simulink for Engg, Oxford Higher Education.								
Reference Books								
1. M. B. Patil, V. Ramanarayanan, V.T. Ranganathan ,“Simulation of Power Electronic Circuits								
Web References:								
1. http://www.digimat.in/nptel/courses/video/108108166/L51.html								
2. https://www.mathworks.com/videos/modeling-and-simulation-of-pv-solar-power-inverters-81813.html								
3. https://www.mathworks.com/videos/developing-dc-dc-converter-control-with-simulink-modeling-simulating-and-sizing-passive-components-1535536730358.html								

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.

SCADA SYSTEMS AND SEQUENCE OF EVENT RECORDING SYSTEM (SCADA)

B.Tech. EEE (Honors) – POOL-4					Scheme : 2020			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEE16	Honors	L	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	2	4	40	60	100
Course Outcomes : At the end of the course the student will be able to								
CO1: The purpose of this course is to understand the Fundamental concept of supervisory control against local control								
CO2: The purpose is to create a mimic diagram of a process and to get a birds eye view of the entire process								
CO3: The purpose is to understand how SCADA helps in improving the process.								
UNIT – I								
Introduction to SCADA system	Introduction to SCADA software and its utilities in a process plants. Brief view of the SCADA software and its features.							
UNIT - II								
Mimic diagram	Creating new project and its work bench properties. Configuring PLC ports, devices and tags. Configuring process screens for Bottling plant using object library. Creating the mimic screens and advantages of the same.							
UNIT – III								
Live trends charts in a mimic diagram	Creating live trends and attaching points from the tag database. Concept of ODBC, OLE.							
UNIT - IV								
Historian function and Data base logger, alarm management	Concept of RDBMS, creating a Data base logger application, configuring, creating historical trend and importing the same in CSV file, creating alarm screens.							
UNIT - V								
Advanced functions in SCADA and Sequence of event recording	Understanding the advanced functions like web server, server redundancy, receipt management. The concept and sequence of event recording and its advantages, time stamping of the data events.							
Text Books								
1. Stuart A. Boyer: „SCADA-Supervisory Control and Data Acquisition“, Instrument Society of America Publications, USA, 1999.								
2. Gordon Clarke, Deon Reynders, „Practical Modern SCADA Protocols: DNP3, 60870.5 and Related Systems“, Newnes Publications, Oxford, UK,2004								
3. Efim Rosenwasser, Bernhard P. Lampe, „Multivariable computer-controlled systems: a transfer function approach“, Springer, 20.								
Reference Books								
1. Gordon Clarke, Deon Reynders, „Practical Modern SCADA Protocols: DNP3, 60870.5 and Related								

Systems“, Newnes Publications, Oxford, UK,2004

2. Stuart A. Boyer,“SCADA-Supervisory Control and Data Acquisition“, Instrument Society of America Publications,USA,2004

3. William T. Shaw, „Cybersecurity for SCADA systems“, PennWell Books, 2006

Web References:

1. <https://www.dpstele.com/scada/how-systems-work.php>

2. <https://www.processsolutions.com/understanding-scada-and-what-it-can-do-for-you/>

3. <https://nptel.ac.in/content/storage2/courses/108106022/LECTURE%201.pdf>

Question Paper Pattern:

Internal Assessment: The question paper for sessional examination shall be for 25 marks, covering half of the syllabus for first sessional and remaining half for second sessional exam. The question paper shall consist of three sections with Two Questions (EITHER/ OR Type) in each section. The student shall answer one question from each section.

End Exam: The question paper for End examination shall be for 60 marks. The Question paper shall contain Five Units with Two Questions (Either or Type) from each unit. Each of these questions may contain sub questions and the student should answer any one question from each unit. Each Question carries 12 marks.