**G. PULLA REDDY ENGINEERING COLLEGE(AUTONOMOUS): KURNOOL**

**Department of Electronics and Communication Engineering**

**IEEE Communications society**

**IEEE Information Theory society**

## CIRCULAR

**Date:24/09/2024**

The Department of Electronics and Communication Engineering ,IEEE Communications society and IEEE Information Theory society is organizing a Three Day National Level workshop "**Exploring VERILOG and FPGA for Digital Design**" during 3rd– 5th October 2024. This workshop includes discussion on various topics such as Digital Design, Introduction to HDL's, Digital Design using XILINX VIVADO- FPGA –ZYNQ 7000 Technology. This workshop also conducts Hands on Session on various EDA Tools for students. In this regard, it is requested to all the students to utilize the opportunity and get benefited. Registration details and Event Schedule are given below:

**Registration Link: http://bit.ly/exploringverilogandfpga**

| S.No | Event Name | Date | Time | Venue | Fee Details |
|---|---|---|---|---|---|
| 1. | **Workshop on "Exploring Verilog and FPGA for Digital Design"** | **3rd to 5thOctober 2024** | **FN - 10:30 AM to 12:20 PM**<br><br>**AN - 1:20 PM to 3:00 PM** | **ECE BLOCK 1**<br><br>**AVLSI LAB** | **Rs.400/- for IEEE Student members**<br>**Rs.450/- for Non-IEEE student members**<br><br>**Rs.500/- for PG student/Research Scholar** |

Further Details Contact

Event Coordinators:

1. Smt.D.Rohini ,Asst.Prof., Dept of ECE–7095667770.
2. Smt.G.Divya Praneetha, Asst.Prof., Dept of ECE –7093812519.

K. Devaki Dee.

Dean of Student Affairs

Enclosure

Brochure of the event

Copy to: All Department Main Notice board's

Website-Incharge

Smt.D.Rohini, Faculty Advisor of IEEE Communications Society, ECE Dept.

Smt.G. Divyapraneetha, Faculty Advisor of IEEE Information Theory Society, ECE Dept.

To be circulated among the ECE students of B.Tech II,III and IV year.

## DEPARTMENT

The ECE dept. was established in the academic year 1984-85. The department has highly qualified faculty having specialized in diversified areas of technology like Communications, Signal Processing, Microelectronics, Microprocessors, Instrumentation and control and Digital Electronics. The department is well equipped and has excellent laboratory facilities. With the idea of "disseminating Knowledge through interaction", department has been organizing National Level Technical Symposiums, Workshops, faculty development programs etc., through the constant support and enthusiasm of the management, faculty and students.

## IEEE

IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity. IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. IEEE will be essential to the global technical community and to technical professionals everywhere, and be universally recognized for the contributions of technology and of technical professionals in improving global conditions.

## WORKSHOP

The aspiration of the workshop is to motivate and to explore through exploring "Verilog and FPGA for Digital Design" for the beneficiary of students to enhance their expertise. The workshop is organized with academic and Industry experts to have the real time experience for the participants. Hands-on-session is provided for effective learning by practitioners. This workshop provides an opportunity to upgrade the technical profile of the participants.

## RESOURCE PERSONS

**Dr.P.Ranga Babu, Ph.D**
**Associate Professor**
**Dept. of ECE**
**IIITDM Kurnool**

**Smt.Jyotshna Mamillapalli**
**Principal Engineer**
**Synopsys, Hyderabad**

**Dr.M.Madhu Sudhan Reddy**
**Assisstant Professor**
**Dept. of ECE**
**GPREC(A) Kurnool**

## CONTENTS OF THE WORKSHOP

- Introduction to HDL's.
- Digital Design using XILINX VIVADO- FPGA -ZYNQ 7000.

## REGISTRATION FEE

UG Students:
For IEEE- Rs 400/-
For non-IEEE-Rs 450/-
PG Students/Research Scholars: Rs 500/-

## ELIGIBILITY

UG Students
PG Students
Research Scholars

**CERTIFICATES WILL BE ISSUED TO ALL THE PARTICIPANTS**

## REGISTRATION LINK

http://bit.ly/exploringverilogandfpga

**DEADLINE:**
**1st October, 2024**

**NOTE: REGISTRATIONS ARE LIMITED TO FEW SEATS ONLY**

## ORGANIZED BY

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING,
IEEE COMMUNICATIONS SOCIETY,
IEEE INFORMATION THEORY SOCIETY

## ORGANIZATION

G.Pulla Reddy Engineering College is the brainchild of Late Sri G.Pulla Reddy, the renowned philanthropist and a great humanist. Established in 1984-85, it is one of the earliest private engineering colleges in Andhra Pradesh state. The college was inaugurated by the world famous ophthalmologist, Padma Bhushan, Dr.P. Siva Reddy on 22nd February, 1985.The college is being managed by G. Pulla Reddy Charities trust, Hyderabad. The college continuously strived with a visionto become the choicest institute of technology and a hub of academic and industrial research and development and worked with a mission to provide conducive academic ambience, excellent infrastructure, continually updated lab equipment and committed and scholarly faculty to realize the vision of the college. GPREC has been functioning as an autonomous institution since 2006. The college has permanent Affiliation to JNTUA, Anantapuramu and is approved by All India Council for Technical Education (AICTE), New Delhi and accredited by NBA of AICTE and NAAC of UGC with A grade.

**CHIEF PATRON**
**Sri.P.SUBBA REDDY**
Chairman,
GPREC(A),KURNOOL.

**PATRON**
**Dr.B.SREENIVASA REDDY**
Principal,
GPREC(A), KURNOOL.

**CO-PATRONS**
**Dr.S.NAGARAJA RAO**
Prof & HOD, Dept of ECE,
GPREC(A), KURNOOL.

**Dr.K.SURESH REDDY**
Prof & Associate Head, Dept of ECE,
GPREC(A), KURNOOL.

**ADVISORY COMMITTEE**
**Dr.V.ANANTHA LAKSHMI**
Branch Counsellor, GPREC SB.

**Dr.G.V.R.SAGAR**
Associate Prof, Dept of ECE,
GPREC(A), KURNOOL.

**COORDINATORS**
**Smt.D.ROHINI**
Asst Professor, Dept of ECE,
GPREC(A), KURNOOL.

**Smt.G.DIVYA PRANEETHA**
Asst Professor, Dept of ECE,
GPREC(A), KURNOOL.

# A THREE DAY NATIONAL LEVEL HANDS ON WORKSHOP ON

# Exploring VERILOG and FPGA for Digital Design

## 3rd - 5th OCTOBER, 2024