G.PULLA REDDY ENGINEERING COLLEGE (Autonomous) :: KURNOOL
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
TIME TABLE for the Academic year 2023-2024 with effect from 25-03-2024
VLSI & Embedded Systems(VLSI & ES)

CLASS : M.Tech - II semester(Scheme-2022) **LECTURE HALL: PG4**

Day / Time	09.30 am - 10.30 am	10.30 am -11.30am	11.45 am -12.45pm		1.30 pm - 2.30pm	2.30 pm - 3.30pm	3.30 pm - 4.30pm
MON	ESIOT smsd	AID kr	CVD mlm	LUNCH BREAK	AESL Lab smsd,mms		
TUE	ESIOT smsd	VDFT mmsr	MESD wy		AEDAL Lab mmsr,gvr		
WED	MESD wy	VDFT mmsr	ESIOT smsd		CVD mlm	AID kr	AID kr
THU	CVD mlm	VDFT mmsr	MESD wy				
FRI	SMY gs		LIB				
SAT							

		Theory:				Faculty Member:
1	AID	Analaog IC Design		---------	kr	Sri K. Raju
2	ESIOT	Embedded Systems	for Internet of Things		smsd	Dr .S.M.Shamsheer Daula
3	CVD	Design	(Professional Elective-III)	---------	mlm	Smt M. Lalitha Meghana
4	MESD	Microcontrollers for Embedded System Design	(Professional Elective-IV)	---------	wy	Smt W.Yasmeen
5	VDFT	VLSI Design For Testability	(Professional Elective-V)	---------	mmsr	Dr. .M.Madhu Sudhan Reddy
6	SMY	Audit Course - II	(Stress Management by Yoga)	---------	gs	Dr G. Shankaraiah
		<u>Practicals</u>				
8	AEDA	Advanced Electronic Design Automation Lab		---------	mmsr,gvrs	Dr.M.Madhu Sudhan Reddy, Dr G.V.R Sagar
9	AESL	Embeded IOT Lab		---------	smsd,mmsr	Dr .S.M.Sha Dr.M.Madhu Sudhan Reddy

epared by : Sri B. Siva Reddy **Verfied by: HOD (E.C.E.)** **Approved by :PRINCIPAL**