G. PULLA REDDY ENGINEERING COLLEGE (Autonomous): KURNOOL

Accredited by NBA of AICTE and NAAC of UGC
An ISO 9001:2008 Certified Institution
Affiliated to JNTUA, Anantapuramu.

M.Tech Syllabus- Scheme 2017

(VLSI and Embedded Systems)

TWO YEAR M.TECH DEGREE COURSE (SCHEME-2017)

Scheme of Instruction and Examination

(Effective from 2017-2018)

M.Tech - I Semester **VLSI and Embedded Systems**

S. No.	Course No.	Course Title	Credits	Scheme of Instruction periods/week			Scheme of Examination		
				L	T	P	End Exam Marks	Internal Assessment Marks	Total Marks
1.	EC851	CMOS Analog IC Design(AICD)	3	3	-	–	60	40	100
2.	EC852	Advanced Digital System Design using Verilog (ADSD)	3	3		–	60	40	100
3.	EC853	Embedded Real Time Operating System (ERTOS)	3	3	-	–	60	40	100
4.	EC854	Advanced Embedded systems (AES)	3	3		–	60	40	100
5		Elective – I	3	3	-	–	60	40	100
6		Elective-II	3	3	-	–	60	40	100
7.	AU101	Technical English	-	2	-	-	-	-	-
8.	EC863	Advanced VLSI and Embedded Systems Lab (AVESP)	2	–	-	3	50	50	100
		Total	**20**	**20**	**-**	**3**	**410**	**290**	**700**

M.Tech - II Semester **VLSI and Embedded Systems**

S. No.	Course No.	Course Title	Credits	Scheme of Instruction periods/week			Scheme of Examination		
				L	T	P	End Exam Marks	Internal Assessment Marks	Total Marks
1	EC951	Low Power VLSI Design(LVD)	3	3	-	–	60	40	100
2	EC952	VLSI Design for Testability (VDFT)	3	3	-	–	60	40	100
3.	EC953	VLSI Architecture (VLSIA)	3	3	-	–	60	40	100
4	EC954	Microcontrollers for Embedded System Design(MESD)	3	3	-	–	60	40	100
5.		Elective – III	3	3	-	-	60	40	100
6.		Elective – IV	3	3	-	-	60	40	100
7.	AU102	Research Methodology(RM)	-	2	-	-	-	-	-
8.	EC963	Advanced Electronic Design Automation Lab (EDAP)	2	-	-	3	50	50	100
		Total	**20**	**20**	**-**	**3**	**410**	**290**	**700**

S. No.	Course No.	Course Title	Credits	Scheme of Instruction periods/week			Scheme of Examination		
				L	T	P	End Exam Marks	Internal Assessment Marks	Total Marks
1.	EC964	Dissertation	12	-	-	-	50	50	100

List of Subjects for Electives

Description	Subject title	Code
Elective-I	CMOS Digital IC Design (DICD)	EC855
	CPLD and FPGA ARCHITECTURES and APPLICATIONS (FPGA)	EC856
	Scripting Languages for VLSI Design Automation (SLA)	EC857
	VLSI Technology (VTECH)	EC858
Elective II	Embedded Programming (EP)	EC859
	Embedded System Architecture (ESA)	EC860
	Robotics and Automation (RAA)	EC861
	Advanced Computer Networks (ACN)	EC862
Elective III	VLSI Signal Processing (VS)	EC955
	Electronic Design Automation Tools (EDAT)	EC956
	System on Chip Architecture (SOCA)	EC957
	Design of Semiconductor Memories(DSM)	EC958
Elective IV	Principles of Distributed Embedded Systems (PDES)	EC959
	Embedded Linux (ELX)	EC960
	Embedded Networks and Protocols (ENP)	EC961
	Hardware Software Co-design (HSC)	EC962

CMOS ANALOG IC DESIGN (AICD)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC851	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: design simple and high impedance current mirror circuits and their frequency response

CO2: design Differential OP-AMP and comparator circuits

CO3: design Sample and hold and switched capacitor circuits

CO4: understand Nyquist rate Data converters

CO5: understand Oversampling Data converters and filters

Basic current mirrors and single stage amplifiers

Simple CMOS current mirror, common source, Common gate amplifier with current mirror active load, Source follower with current mirror to supply bias current, High output impedance current mirrors and bipolar gain stages, Frequency response.

Operational amplifier design and compensation

Two stage CMOS operational amplifier. feedback and operational amplifier compensation, advanced current mirrors, Folded-cascode operational amplifier, Current mirror operational amplifier, Fully differential operational amplifier, common mode feedback circuits, Current feedback operational amplifier. Comparator, Charge injection error, Latched comparators, BiCMOS comparators.

Sample and hold and switched capacitor circuits

MOS, CMOS and BiCMOS sample and hold circuits, Switched capacitor circuits, Basic operation and analysis, first order and biquad filters, Charge injection, Switched capacitor gain circuit, Correlated double sampling techniques, Other switched capacitor circuits.

Data converters

Ideal D/A and A/D converters, Quantization noise, Performance limitations. Nyquist rate D/A converters, Decoder based converters, Binary scaled converters, Hybrid Converters, Nyquist rate A/ D converters, Integrating, Successive approximation, Cyclic flash type, Two step, interpolating, Folding and pipelined A/D converters.

Over sampling converters and filters

Over sampling with and without noise shaping, Digital decimation filter, High order modulators, Band pass over sampling converters, Practical Considerations, Continuous time filters, first order and second order filters, introduction to G_m-c filters.

Text Books :

1. Paul. R. Gray & Robert G. Major, Analysis and Design of Analog Integrated Circuits, John Wiley & sons, 2004.
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004.
3. P.E. Allen, D.R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2002

Reference Books :

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill. 2002.
2. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.
3. Mohamed Ismail, Analog VLSI, McGraw hill, 1st Edition, 1994.

Web References:
1. http://nptel.ac.in/courses/117106030/35
2. https://link.springer.com/chapter/10
3. http://www.ee.iitm.ac.in/videolectures/doku.php?id=ee658_2008
Question Paper Pattern:
Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions **End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ADVANCED DIGITAL SYSTEM DESIGN USING VERILOG (ADSD)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC852	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3		-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Analyze and design sequential digital circuits

CO2: Analyze and design asynchronous sequential digital circuits

CO3: Design using programmable logic devices

CO4: Identify the requirements and specifications of the system required for a given application

CO5: Design and use programming tools for implementing digital circuits of industry standards

SEQUENTIAL CIRCUIT DESIGN

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

SYSTEM DESIGN USING VERILOG

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

Text Books :

2. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004

3. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001

Reference Books :

1. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002

2. Parag K.Lala “Digital system Design using PLD” B S Publications,2003

3. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.

4. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

EMBEDDED REAL TIME OPERATING SYSTEM (ERTOS)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC853	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand Real Time Systems and RTOS functionality

CO2: Understand the UNIX file system and its Programming

CO3: Understand the VxWorks, Posix, µC/OS-II and RT Linux environments

CO4: Understand the debugging tools for suitable RTOS Environments

Concept of Embedded Operating Systems

Differences between Traditional OS and RTOS. Real Time Systems. RTOS Kernel & Process Management. Create, Ready, Run, Interrupt, Wait and Terminate States. Intertask Communication & Synchronization, Context Switching.

Interprocess Communication (IPC):

Hard Real-time systems, Soft Real-time systems. Classical Uniprocessor Scheduling Algorithms, RMS, Preemptive EDF. IPC through Semaphores, Mutex , Mailboxes, Message Queues or Pipes and Event Flags.

UNIX Operating Systems

UNIX Kernel, File system, Concepts of, Process, Concurrent Execution & Interrupts. Process Management, forks & execution. Programming with system calls, Process Scheduling, Shell programming and filters.

RTOS Environments

POSIX Real Time Extensions, Software Logic Analyzers, ICEs. Comparison of RTOS, VxWorks, µC/OS-II and RT Linux for Embedded Applications.

Debugging Tools

OTP emulators, On board emulation of Software using Cross Development Environments, Software Logic Analyzers, ICEs.

Text Books :

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

2. Operating System Concepts – Silberschatz, Galvin and Gagne, 8th Edition ©2009

Reference Books :

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.

2. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

3. MicroC/OS-II, Jean.J.Labrosse, 2nd Edition,Elsevier, 2012, CMP Books

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ADVANCED EMBEDDED SYSTEMS (AES)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC854	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand Intel 8051 and Atmel microcontrollers features for embedded systems

CO2: Utilize the programming model of 8051 microcontroller in framing various programs.

CO3: Understand the Embedded C programming techniques for microcontrollers.

CO4: Use Embedded C in interfacing of I/O peripherals to microcontrollers

Introduction to embedded systems

Background and History of Embedded Systems, Definition and Classification, Programming languages for embedded systems. **Processor and Memory Organization:** Structural units in processor, Processor selection for an embedded system, Memory devices, Memory selection, Allocation for memory to program segments and blocks and memory map of a system.:

8051 Microcontroller and operations

Microprocessors Vs Microcontrollers, 8051 Family, Architecture, Pin Functions, Addressing Modes, Instruction Set. The external interface of the Standard 8051, Memory issues, I/O pins, Timers, Interrupts, Serial interface.

Programming Structure

Programs using 8051 instruction set. Introduction to embedded C, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version). Example: Reading switch inputs (basic code), Example: Counting goats

Adding Structure to the Code

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

Meeting Real-Time Constraints

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2. The need for 'timeout' mechanisms, Creating loop timeouts. Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout.

Text Books :

1. *Embedded C* by **Michael J. Pont**, A Pearson Education, 1st Edition, 2002.
2. *Embedded Systems Architecture, Programming and Design*, by Raj Kamal 2nd Edition, TMH, 2006.

Reference Books :

1. *An Embedded Software Primer*, by David.E. Simon 2nd Edition, Pearson Edition, 2009.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

TECHNICAL ENGLISH (TE)

I Semester: Common for All M.Tech Programmes					Scheme: 2017			
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
AU101	**Audit Course**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
		2	**-**	**-**	**-**	**-**	**-**	**-**
Sessional Exam Duration: -					**End Exam Duration: -**			

Course Outcomes: At the end of the course students will be able to

CO 1: write Technical Reports, Journal Papers and Project Reports.

CO 2: write Job Applications, Resumes and Statements of Purpose.

Course Content

1. Technical Reports –Formats and Styles
   a) Feasibility Report
   b) Factual Report
   c) Project Reports
2. Journal Papers- Formats
3. Paper Presentation Strategies
4. Statement of Purpose for Internships and Apprenticeships
5. Letter Writing- Job Applications, Resume Preparation
6. Common Errors in Research Papers

Reference Books:

1. Sangeeta Sharma & Binod Mishra, Communication Skills for Engineers and Scientists, PHI Learning Private Limited.
2. M. Ashraf Rizvi, Effective Technical Communication, Tata McGraw-Hill Publishing Company Ltd., 2005.
3. Thomas S. Kane , The Oxford Essential Guide to Writing, OUP, 2010
4. Joan van Emden, A Guide to Technical Report Writing http://scisweb.ulster.ac.uk/~projects/guide-to-technical-writing-1.pdf

ADVANCED VLSI AND EMBEDDED SYSTEMS LAB (AVESP)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC863	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	-	-	3	2	50	50	100

End Exam Duration: 3 Hrs

Course Outcomes : At the end of the course the student will be able to

CO1: Understand HDL programming models.

CO2: Design various digital circuits using CPLD and FPGA devices

CO3: Synthesize various Digital circuits.

CO4: Program MSP 430 and Cortex M4 Processors

LIST OF EXPERIMENTS

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.
7. Microcontroller programming using MSP430 and Cortex M4 processors
   a) Toggling the LEDs,
   b) Master Slave Communication,
   c) PWM interface
   d) Sensor Interfacing (Temperature)

Internal Assessment: 50M

End Exam:50M

LOW POWER VLSI DESIGN (LVD)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC951	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand different sources of power dissipation

CO2: Understand minimization of switched capacitance

CO3: Analyze and minimize dynamic and static power consumption in VLSI circuits

CO4: Understand working principles of adiabatic logic

CO5: Find ways to minimize power in software design

Sources of Power Dissipation

Short-Circuit Power Dissipation, Switching Power Dissipation, Glitching Power Dissipation, Leakage Power Dissipation; Power Sources- for low power circuits---chargeable and disposable batteries, **Supply Voltage Scaling for Low Power**: Device Feature Size Scaling, Architectural-Level Approaches, Voltage Scaling Using High-Level Transformations, Multilevel Voltage Scaling, Challenges in MVS, Dynamic Voltage and Frequency Scaling, Adaptive Voltage Scaling, Subthreshold Logic Circuits

Switched Capacitance Minimization

System-Level Approach: Hardware–Software Codesign, Transmeta's Crusoe Processor, Bus Encoding, Clock Gating, Gated-Clock FSMs, FSM State Encoding, FSM Partitioning, Operand Isolation, Precomputation, Glitching Power Minimization, Logic Styles for Low Power: Static CMOS Logic, Dynamic CMOS Logic, PTL; Some Related Techniques for Dynamic Power Reduction

Leakage Power Minimization

VTCMOS Approach, Transistor Stacking, MTCMOS Approach, Power Gating, Isolation Strategy, Sleep transistor, State Retention Strategy, Dynamic Vth Scaling

Adiabatic Logic Circuits

Adiabatic Charging, Adiabatic Amplification, Adiabatic Logic Gates, Pulsed Power Supply, Stepwise Charging Circuits

Low-Power Software Approaches

Introduction, Machine-Independent Software Optimizations, Combining Loop Optimizations with DVFS: *Loop Unrolling , Loop Tiling, Loop Permutation, Strength Reduction, Loop Fusion, Loop Peeling, Loop Un switching*

Text Books :

1. Pal, Ajit, *Low-Power VLSI Circuits and Systems*, Springer,2015

Reference Books :

1. J. Rabaey, *Low Power Design Essentials*, 1st Edition, Springer, 2010

2. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, *Low Power Methodology Manual for System-On-Chip Design*, Springer,2007

3. Christian Piguet, *Low Power CMOS Circuits Technology, Logic Design and CAD Tools*, 1st Indian Reprint, CRC Press, 2010

4. Kaushik Roy and Sharat Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley Inter-science Publications, 2000

Web References:
1. nptel.ac.in/courses/106105034/
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/
3. www.ece.ucdavis.edu/~vojin/CLASSES/EEC280/.../Low-PowerDesignTechniques.pps
Question Paper Pattern:
Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions **End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

VLSI DESIGN FOR TESTABILITY (VDFT)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC952	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand all the levels of testing done in VLSI circuits

CO2: Understand the DFT principles in VLSI circuits

CO3: Understand logic and fault simulation in VLSI circuits

CO4: Generate test generation in VLSI circuits

Introduction to Testing

Importance of Testing, Testing During the VLSI Lifecycle, Challenges in VLSI Testing- Challenges in VLSI Testing, Fault Models; Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology

Design for Testability

Introduction, Testability Analysis----SCOAP Testability Analysis, Probability-Based Testability Analysis, Simulation-Based Testability Analysis; Design for Testability Basics--- Ad Hoc Approach, Structured Approach; Scan Cell Designs--Muxed-D Scan Cell, Clocked-Scan Cell, LSSD Scan Cell; Scan Architectures --- Full-Scan Design, Partial-Scan Design, Random-Access Scan Design; Scan Design Rules, Scan Design Flow diagram and brief description of each stages only, RTL Design for Testability

Logic and Fault Simulation

Logic Simulation for Design Verification, Fault Simulation for Test and Diagnosis, Simulation Models--- Gate-Level Network, Logic Symbols, Logic Element Evaluation, Timing Models; Logic Simulation, Fault Simulation--- serial, parallel, deductive, concurrent and differential fault simulation; fault detection, comparison of Fault Simulation Techniques, Alternatives to Fault Simulation

Test Generation

Introduction, Random Test Generation, Boolean difference, untestable faults, Designing a Stuck-At ATPG for Combinational Circuits--- A Naive ATPG Algorithm, A Basic ATPG Algorithm, D Algorithm, PODEM, PODEM; Designing a Sequential ATPG--- Designing a Sequential ATPG, 5-Valued Algebra Is Insufficient, Gated Clocks and Multiple Clocks; Untestable Fault Identification, ATPG for Non-Stuck-At Faults--- Designing an ATPG That Captures Delay Defects, ATPG for Transition Faults.

Logic Built-In Self-Test

Introduction, Test Pattern Generation--- Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing; Output Response Analysis--- Ones Count Testing, Transition Count Testing, Signature Analysis, Logic BIST Architectures ---- BIST Architectures for Circuits without Scan Chains, BIST Architectures for Circuits with Scan Chains, BIST Architectures Using Register Reconfiguration, BIST Architectures Using Concurrent Checking Circuits, Fault Coverage Enhancement, BIST Timing Control

Text Books :

1. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, “VLSI Test Principles and Architectures: Design for Testability”, 1st Edition, Morgan Kaufmann, 2006.

Reference Books :

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers, 2000
2. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002
3. Parag K. Lala, “Digital Circuits Testing and Testability”, Academic Press Inc, 1997
Web References:
1. http://booksite.elsevier.com/9780123705976/
2. https://onlinecourses.nptel.ac.in/noc17_ec02/preview
3. http://nptel.ac.in/courses/106103116/
Question Paper Pattern:
Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions **End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

VLSI ARCHITECTURES (VLSIA)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC953	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Students will be in position to choose processor architecture for their projects.

CO2: Students will be able to work with DSP processors and understand MAC architecture.

CO3: Students will be able learn advanced concepts in super scalar architectures.

Complex Instruction Set Computers (CISC)

Instruction Set, Characteristics and Functions, Addressing Modes, Instruction Formats, Architectural Overview, Processor Organization, Register Organization, Instruction Cycle, Instruction Pipelining, Pentium Processor, PowerPC Processor

Reduced Instruction Set Computers (RISC)

Instruction execution Characteristics, Register Organization, Reduced Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview, RISC Pipelining, Motorola 88510, MIPS R4650, RISC Vs. CISC

DSP Processors

Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview

Pipeline Processing

Basic Concepts, Classification of Pipeline Processors, Instruction and Arithmetic Pipelining, Design of Pipelined Instruction Units, Pipelining Hazards and Scheduling, Principles of Designing Pipelined Processors

Super Scaler Processors

Overview, Design Issues, PowerPC, Pentium

Text Books :

1. B.Venkatramani & M.Baskar, *Digital Signal Processor*, McGraw Hill, 2000

2. Avatar Singh and S.Srinivasan, *Digital signal processing*, Thomson Books, 2004

Reference Books :

1. K.Hwang & F.A.Briggs, *Computer Architecture and Parallel Processing*, Mc Graw Hill.

2. J.P.Hayes, *Computer Architecture and Organization*, Mc Graw Hill.

3. Dezso Sima, Terence Fountain, Peter Kacsuk, *Advanced Computer Architectures-A Design Space Approach*, Addison-Wiley.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN (MESD)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC954	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand ARM Architecture and pipelining.

CO2: Understand ARM processor instruction set and thumb formats

CO3: Use ARM programming model to frame programs

CO4: Understand the memory management and cache issues of ARM processor

ARM Architecture

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

ARM Programming Model – I

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions..

ARM Programming Model – II

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

ARM Programming

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

Memory Management

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Text Books :

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.
2.

Reference Books :

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

RESEARCH METHODOLOGY (RM)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
AU102	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	-	-	-	-
Sessional Exam Duration : 2 Hrs					End Exam Duration: -		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand overview of research process, state the research problem and conduct a literature review of the concepts comprising the research questions.

CO2: Study the data collection methods and process the data statistically.

CO3: Understand the basic properties of estimators, analyse the estimated data and interpret the data in a research paper.

Meaning, Objective and Motivation in Research

Types of Research, Research Approaches, Research Process, Validity and Reliability in Research. Features of Good Design, Types of Research Design, Basic Principles of Experimental Design, Steps in Sampling Design, Characteristics of a Good Sample Design, Random Samples and Random Sampling Design.

Measurement and Scaling Techniques

Errors in Measurement, Tests of Sound Measurement, Scaling and Scale Construction Techniques, Forecasting Techniques, Time Series Analysis, Interpolation and Extrapolation.

Methods of Data Collection

Primary Data, Questionnaire and Interviews, Collection of Secondary Data, Cases and Schedules.

Statistical Processing

Correlation and Regression Analysis, Method of Least Squares, Regression Vs. Correlation, Correlation Vs. Determination, Types of Correlation and Their Specific Applications.

Hypothesis Testing

Tests of Hypothesis, Parametric Vs. Non-Parametric Tests, Procedure for Testing Hypothesis, Use of Statistical Techniques for Testing Hypothesis, Sampling Distribution, Sampling Theory Chi-Square Test, Analysis of Variance and Covariance, Multivariable Analysis

Interpretation of Data

Data interpretation, Layout of a Research Paper, Techniques o f Interpretation.

Text Books / Reference Books :

1. C.R. Kothari, *Research Methodology (Methods & Techniques)*, New Age International Publishers.
2. R.Cauvery, V.K.Sudha Nayak, M.Girija, Research Methodology, S.Chand Publishers.

ADVANCED ELECTRONIC DESIGN AUTOMATION LAB (AEDAP)

II Semester :VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC963	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	-	-	3	2	50	50	100

End Exam Duration: 3 Hrs

Course Outcomes : At the end of the course the student will be able to

CO1: Perform transient, AC and DC analysis of CMOS based circuits

CO2:.Perform transient, AC and DC analysis of PASS-transistor based circuits

CO3: Perform transient, AC and DC analysis of Transmission Gate based circuits

CO4: Perform transient, AC and DC analysis of circuits like CS,CG,CD, Diff Amplifier, Op-Amp etc.

CO5: Perform DRS,LVS, Layouts of simple circuits.

LIST OF EXPERIMENTS

1. Transient Analysis of various CMOS based circuits (from simple circuits like Inverter to complex circuits like arithmetic circuits).
2. Transient Analysis of PASS Transistor based circuits
3. Transient Analysis of various Transmission Gate (TG) based circuits (eg. XOR gate, MUX etc).
4. Transient, AC, DC Analysis of various amplifier circuits (e.g. CS, CD, Differential, Operational Amplifiers etc.). Finding CMRR (for Differential and Operational Amplifiers) and Bandwidth.
5. Applications based on operational amplifiers (e.g. DAC etc.)
6. DRC, LVS, Parasitic Values Estimation from Layout of CMOS based circuits.

Reference Books :

1. Neil Weste, David Harris, “CMOS VLSI Design, 4th Edition”, Pearson, 2010
2. Paul.R. Gray & Robert G. Major, “Analysis and Design of Analog Integrated Circuits”, John Wiley & sons, 2004
3. David Johns, “Ken Martin, Analog Integrated Circuit Design”, John Wiley & sons. 2004

Internal Assessment: 50M

End Exam:50M

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN (DICD)

I Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC855 (Elective-I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Revise the MOS transistor theory

CO2: Solve various delays in combinational circuit and its optimization methods

CO3: Understand circuit design of latches and flip-flops.

CO4: Understand combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.

CO5: Understand Design Methodology and Tools

MOS Transistor Theory Review

Introduction, Long-Channel I-V Characteristics, C-V Characteristics: Simple MOS Capacitance Models, Detailed MOS Gate Capacitance Model; Non-ideal I-V Effects: Mobility Degradation and Velocity Saturation, Channel Length Modulation, Threshold Voltage Effects, Leakage, Temperature Dependence; DC Transfer Characteristics

Combinational network delay

Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis

Sequencing static circuits

Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

Data path and array subsystems

Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Design Methodology and Tools

Introduction, Structured Design Strategies using with the help of Software Radio Example, Design Methods, Design Flows

Text Books :

1. Neil Weste, David Harris, “CMOS VLSI Design, 4th Edition”, Pearson, 2010

Reference Books :

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic,”Digital Integrated Circuits”, 2nd edition, Pearson Education, 2003
2. W.Wolf, “FPGA- based System Design”, Pearson, 2004.
3. C.Roth,” Fundamentals of Digital Logic Design”, Jaico Publishers, V ed., 2009. 6. Recent literature in Digital System Design

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (FPGA)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC856 (Elective-I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand ROMs, PALs, PLAs, CPLDs

CO2: Get exposure to industry standard FPGAs of XILINX, ALTERA and ACTEL in terms of programming technology, logic block implementation, interconnect structures, and their I/Os.

CO3: Understand the concepts of ASICs and its design Flow

CO4: Understand System partitioning, floor-planning Placement & Routing and associated algorithms

CPLD

Programmable logic, Programmable read only memory (PROM), programmable logic array (PLA), Programmable array logic (PAL). Sequential programmable logic devices (SPLDS), Programmable gate arrays (PGAS), CPLD

FPGA Programming Technology

Programmable logic FPGA general structure, Anti fuse - Static RAM: EPROM and EEPROM technology, PREP benchmarks, FPGA Logic block – Actel ACT - Xilinx LCA, Altera FLEX, Altera MAX;

FPGA I/Os

DC & AC inputs and outputs, Clock and Power inputs, Xilinx I/O block

FPGA Interconnect

Actel ACT -Xilinx LCA - Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX 9000, Altera FLEX,, FPGA Design flow

ASIC Construction

Physical Design ,Goals and objectives of all the ASIC physical design steps, System partitioning, Partitioning method—Constructive partitioning, iterative partitioning, K-L algorithm, Floor planning ,Floor planning tools ,Placement , placement Methods, Placement types-- constructive: min-cut placement method, eigenvalue placement algorithm, Iterative Placement Improvement, Physical design flow.

ASIC Routing

Global Routing : Goals and Objectives , Measurement of Interconnect Delay ,Global routing Methods, Detailed routing: Goals and objectives, Measurement of channel density, Left Edge Algorithm, Circuit Extraction and DRC, Special Routing : Clock Routing and Power Routing .

Text Books :

1. Michael John Sebastian Smith, *Application specific Integrated Circuits*, 3rd Edition, Pearson Education Asia, 2001.

2. Pak and Chan, Samiha Mourad, *Digital Design using Field Programmable Gate Arrays*, 1st Edition Pearson Education, 2009.

Reference Books :

1. S. Trimberger, Edr, *Field Programmable Gate Array Technology*, 1st Edition Kluwer Academic Publications,1994.

2. John V.Oldfield, Richard C Dore, *Field Programmable Gate Arrays*, 1st Edition,Wiley Publications, 1999.

3. S. Brown, R. Francis, J. Rose, Z.Vransic, *Field Programmable Gate array*, 1st Edition, Kluwer Publications, 1992.

Web References:
1. http://www.fpgacenter.com/
2. http://www.cpld.com/
3. www.asic.co.in/
Question Paper Pattern:
Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions **End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

SCRIPTING LANGUAGES FOR VLSI DESING AUTOMATION (SLA)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC857 (Elective-I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Students are capable of scripting the given code in HDLs.

CO2: Students will get benefit of using Scripting languages in their projects.

CO3: Students will get scope for learning Java Script, SKILL etc.

Overview of scripting languages

PERL, File handles, Operators, Control structures, Regular expressions, Built in data types, Operators, Statements and declarations- simple, Compound, Loop statements, Global and scoped declarations.

Pattern matching

Regular expression, Pattern matching operators, Character classes, Positions, capturing and clustering.

Subroutines

Syntax, Semantics, Proto types, Format variables, References, Data structures, Arrays of arrays, Hashes of arrays, Hashes of functions, Inter process communication, Signals, Files, Pipes, sockets.

Threads

Process model, Thread model, Perl debugger, Using debugger commands, Customization, Internals and externals, Internal data types, Extending perl, embedding perl, Exercises for programming using perl.

Other languages

Broad features of other scripting languages SKILL, CGI, java script, VB script

Text Books / Reference Books :

1. Larry Wall, Tom Christiansen, John Orwant, *Programming perl*, 3rd Edition, Oreilly publications

2. Randal L, Schwartz Tom Phoenix, *Learning PERL*, Oreilly publications

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

VLSI TECHNOLOGY (VTECH)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC858 (Elective-I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: understand the MOS technologies, its models and latch-up problem

CO2: understand the layout design and layouts of logic gates

CO3: understand all the stages of manufacturing an IC

CO4: understand the doping and deposition concepts

CO5: understand design rules and scaling, BICMOS ICs in

Review of Microelectronics and Introduction to MOS Technologies

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

Layout Design

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

Stages of Manufacturing

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

Doping and depositions

Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitaxy, molecular beam epitaxy

Design rules and Scaling, BICMOS ICs

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

Text Books :

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997

2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 20000

Reference Books :

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning 2011

2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999

3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000

4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

EMBEDDED PROGRAMMING (EP)

I Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC859 (Elective-II)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand C language and assembly programming.

CO2: Understand Object orientation for programming and C++.

CO3: Understand software modeling fundamentals.

CO4: Understand Embedded software development tools

INTRODUCTION TO ASSEMBLY LANGUAGE AND DATAREPRESENTATION IN C

Assembly language programming – macros - Data repre sentation – Twos complement, fixed point and floating point number formats –Low level programming in C: Primitive data types – Pointers – Structures – Unions – Dynamic memory allocation – Functions – recursive f unctions - Linked lists.

PROGRAMMING IN C

Register usage conventions – Typical use of addressing options – Instruction sequencing – Procedure call and return – Functions – recursive functions – 8, Parameter passing – Retrieving parameters – Everything in pass by value – Temporary variables – threads – preemptive kernels – system timer – scheduling

OBJECT ORIENTED PROGRAMMING

Object oriented analysis and design - C++ classes and objects – functions – data structures - examples

UNIFIED MODELING LANGUAGE

Connecting the object model with the use case model – Key strategies for object identification – UML basics. Object state behavior – UML state charts – Role of scenarios in the definition of behavior – Timing diagrams – Sequence diagrams – Event hierarchies – types and strategies of operations – Architectural design in UML concurrency design – threads in UML

EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS

The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS

Text Books :

1. David E. Simon, " *An Embedded Software Primer*", Pearson Education, 2003.
2. Daniel W. Lewis, " *Fundamentals of embedded software where C and assembly meet*", Pearson Education, 2002.

Reference Books :

1. Steve Heath, " *Embedded system design*", Elsevier, 2003.
2. E. Balaguruswamy, " *Object oriented programming with C++*", Tata McGraw Hill, 2011.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

EMBEDDED SYSTEM ARCHITECTURE (ESA)

I Semester : VLSI & ES				Scheme : 2017			
Course Code	Hours/Week			Credits	Maximum Marks		
EC860 (Elective-II)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	0	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand the Embedded System Models

CO2: Understand the typical engineering issues of software development.

CO3: Understand rationale and concepts for designing embedded systems

CO4: Analyze the Embedded Issues of Software

Introduction to embedded systems

Embedded system model – embedded standards – block diagrams – powering the hardware - embedded board using Von Neuman model. Embedded processors: ISA architecture models – application specific ISA models – general purpose ISA models – instruction level parallelism.

Processor Hardware

Internal processor design: ALU – registers – control unit - clock – on chip memory – processor i/o – interrupts – processor buses – processor performance.

Support Hardware

Board memory: ROM – RAM – cache – auxiliary memory – memory management – memory performance – board buses: arbitration and timing – PCI bus example – integrating bus with components – bus performance.

Software

Middleware and applications: PPP – IP middleware – UDP – Java . application layer: FTP client – SMTP – HTTP server and client.

Engineering Issues Of Software

Design and development: architectural patterns and reference models – creating the architectural structures – documenting the architecture – analyzing and evaluating the architecture – debugging testing, and maintaining.

Text Books :

1. *Embedded system architecture*, Tammy Noergaard, Elsevier, 2006.

Reference Books :

1. *Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C*, Jean J. Labrosse, The publisher, Paul Temme, 2011.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ROBOTICS AND AUTOMATION (RAA)

I Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
ECE861 (Elective-II)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	0	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand anatomy and laws of robotics

CO2: Understand the micro machines and types of the control modes.

CO3: Understand the forward kinematics and its techniques.

CO4: Use robot programming tools in robot cell design

Basic Concepts

Definition and origin of robotics – different types of robotics – various generations of robots – degrees of freedom – Asimov's laws of robotics –anatomy of robot- applications of robots.

Power Sources And Sensors

Hydraulic, pneumatic and electric drives – determination of HP of motor and gearing ratio – variable speed arrangements – path determination – micro machines in robotics – machine vision – ranging – laser – acoustic – magnetic, fiber optic and tactile sensors.

Manipulators, Actuators And Grippers

Construction of manipulators – manipulator dynamics and force control –types of control modes- electronic and pneumatic manipulator control circuits – end effectors – various types of grippers.

Kinematics And Path Planning

Forward kinematics-solution of inverse kinematics problem – multiple solution jacobian work envelop – hill climbing techniques – robot programming languages

Case Studies

Mutiple robots – machine interface – robots in manufacturing and non- manufacturing applications – robot cell design – selection of robot.

Text Books :

1. *Introduction to Robotics Analysis, Systems, Applications*, Saeed B. Niku, Prentice Hall of India/PearsonEducation, Asia, 2001.
2. *Industrial Robots - Technology Programming and applications*, Mikell P. Groover, et.al McGraw Hill, 1980.

Reference Books :

1. *Robotics for Engineers*, Yoran Koren, McGraw Hill. 1980
2. *Introduction to Robotics Mechanics and Control* , Craig, Second edition, Pearson Education, Asia, 2004.
3. *Robotics Technology and Flexible Automation*, Satya Ranjan Deb, TMH, New Delhi, 2001

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ADVANCED COMPUTER NETWORKS (ACN)

I Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC862 (Elective-II)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	0	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand Intel 8051 and Atmel microcontrollers features for embedded systems

CO2: Utilize the programming model of 8051 microcontroller in framing various programs.

CO3: Understand the Embedded C programming techniques for microcontrollers.

CO4: Use Embedded C in interfacing of I/O peripherals to microcontrollers

Congestion and Quality of Service (QoS)

Data traffic, Congestion, Congestion Control, Open loop and Closed Loop Congestion Control in TCP and Frame Relay, Quality of Service, Flow Characterization, Flow Classes, Need For QoS, Resource Allocation, Best Effort Service Features, Techniques to Improve QoS. Queue Management: Passive, Active (RED), and Fair (BRED, Choke) Queue Management Schemes, Scheduling, Traffic Shaping, Resource Reservation and Admission Control Scheduling, Integrated and Differential Services.

Wireless Local Area Networks

Introduction, Wireless LAN Topologies, Wireless LAN Requirements, the Physical Layer, the Medium Access Control (MAC) Layer, Latest Developments. Wireless Personal Area Networks (WPANs): Introduction to PAN Technology and Applications, Commercial Alternatives- Bluetooth, Home RF. Wireless Wide Area Networks and MANS: The Cellular Concept, Cellular Architecture, The First-Generation Cellular Systems, The Second- Generation Cellular Systems, The Third- Generation Cellular Systems, Wireless in Local Loop, Wireless ATM, IEEE 802.16 Standard.

Cellular Systems and Infrastructure

Based Wireless Networks: Cellular Systems Fundamentals, Channel Reuse, SIR and User Capacity, Interference Reduction Techniques, Dynamic Resource Allocation, Fundamental Rate Limits. Virtual Private Network (VPN): Types of VPN, VPN General Architecture, Current VPN Advantages and Disadvantages, VPN Security Issues, VPN Standards.

ATM Protocol Reference Model

Introduction, Transmission Convergence (TC) Sub-layer, Physical Medium Dependent (PMD) Sub-layer, Physical Layer Standards for ATM. ATM Layer: ATM Cell Header Structure at UNI, ATM Cell Header Structure at NNI, ATM Layer Functions. ATM Adaptation Layer: Service Classes and ATM Adaptation Layer, ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 2 (AAL2), ATM Adaptation Layer 3/4 (AAL3/4), ATM Adaptation Layer 5 (AAL5). ATM Traffic and Service Parameterization: ATM Traffic Parameters, ATM Service Parameters, Factors Affecting QoS Parameters, ATM Service Categories, QoS and QoS Classes.

Interconnection Networks

Introduction, Banyan Networks- Properties, Crossbar Switch, Three Stage Class Networks, Rearrangeable Networks, Folding Algorithm, Benes Networks, Looping Algorithm, Bit- Allocation Algorithm. SONET/SDH: SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks

Text Books :

1.Wireless Communications - Andrea Goldsmith, 2005, Cambridge University Press.

2. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.

3. Data Communication and Networking - B. A.Forouzan, 2nd updating, 2004,TMH

Reference Books :
1.Introduction to Broadband Communication Systems- Sadiku, Mathew N.O., Akujuobi, Cajetan.M, PHI
2. Wireless Networks- P. Nicopolitidis, A. S. Pomportsis, G. I. Papadimitriou, M. S. Obaidat, 2003, JohnWiley & Sons.
Question Paper Pattern:
Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions **End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

VLSI SIGNALPROCESSING (VS)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC955 (Elective-III)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Apply the principles of DFG in DSP architectures.

CO2: Apply pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.

CO3: Solve Register minimization, retiming, folding techniques for the given digital filter.

CO4: Understand the overview FIR filter Systolic architecture design.

Introduction to Digital Signal Processing Systems

Introduction, Typical DSP Algorithms, DSP Application demands and scaled CMOS technologies, Representation of DSP Algorithms.

Iteration Bound

Introduction, Data Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs.

Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power.

Retiming and Unfolding

Introduction, Definitions and properties, Solving systems of inequalities, Retiming Techniques, An algorithm for unfolding, Critical path, Unfolding and retiming, Applications of unfolding.

Folding

Introduction, Folding techniques, Register minimization techniques, Register minimization in folded architecture, Folding of multirate systems.

Systolic Architecture Design

Introduction, System array design methodology, FIR systolic arrays, selection of scheduling vector, Matrix-matrix multiplication and 2-D systolic array design, Systolic Design for space representations containing delays.

Text Books :

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science. 1998.

2. Kung S. Y, H. J. While House, T. Kailath, *VLSI and Modern Signal processing*, Prentice Hall, 1985.

Reference Books :

1. Jose E. France, Yannis Tsividis, Design of Analog, Digital VLSI Circuits for Telecommunications and Signal Processing, Prentice Hall,1994.

2. Medisetti V. K , *VLSI Digital Signal Processing* , IEEE Press (NY), USA, 1995.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ELECTRONIC DESIGN AUTOMATION TOOLS (EDAT)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC956 (Elective-III)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Utilize EDA tools in their projects**.**

CO2: Design synthesizable verilog code.

CO3: Explain the difference between verilog and systemverilog and write SystemVerilog code.

CO4: Design circuits using Pspice.

Synthesis and simulation using HDLs

Logic synthesis using verilog. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

Circuit commands for simulation using Spice

Circuit description AC, DC and transient analysis, Advanced spice commands and analysis-SUBCKT, ENDS, FUNC, GLOBAL, INC, LIB, NODESET, options, PARAM, Fourier analysis, Noise Analysis, SENS, STEP, DC.

Circuit simulation using Spice

Models for diodes, transistors and opamp. Digital logic circuits-digital gates and timing models, flip flops and latches.

Data Types in SystemVerilog

Introduction, data types-Built-In Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Array Methods, Choosing a Storage Type, typedef, User-Defined Structures, Packages, Type Conversion, Streaming Operators, Enumerated Types, Constants, Strings.

Design of Procedures, routines and basic test benches in SystemVerilog

Procedural Statements, Tasks, Functions, and Void Functions, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values. Basic Testbench Design- Separating the Testbench and Design, The Interface Construct.

Text Books :

1. M.J.S.Smith, Application Specific Integrated Circuits,Pearson,2002.
2. M.H.Rashid, Spice for Circuits and Electronics using Pspice. (2/e), PHI.
3. Chris Spear_and_Greg Tumbush,SystemVerilog for Verification,3/e,Springer.

Reference Books :

1. S.Sutherland, S. Davidmann, P. Flake, “System Verilog For Design”,(2/e), Springer,2006.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

SYSTEM ON CHIP ARCHITECTURE (SOCA)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC957 (Elective-III)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: understand system approach for SoC design

CO2: understand processor design as part of SoC design

CO3: understand Memory design as part of SoC design

CO4: understand interconnect optimization and configuration in an SoC

CO5: understand applications of SoC with the help of case studies

Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

Processors

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors

Memory Design for SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

Interconnect Customization and Configuration

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Application Studies / Case Studies

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books :

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd

2. ARM System on Chip Architecture - Steve Furber - 2nd Ed., 2000, Addison Wesley Professional

Reference Books :

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM

3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

DESIGN OF SEMICONDUCTOR MEMORIES (DSM)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC958 (Elective-III)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Students will get insight into basic memory techniques to advanced memory techniques.

CO2: Students will be able to analyze faults in memories.

CO3: Students will be able to use efficient memory techniques in their projects especially testing phase.

SRAM Cell Structures

MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies, Silicon On Insulator (SOl) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs

DRAM Technology Development

CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS, DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

Masked Read-Only Memories (ROMs)

High Density ROMs, Programmable Read-Only Memories (PROMs)-Bipolar PROMs, CMOS PROMs-Erasable (UV), Programmable Road-Only Memories (EPROMs), Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs, Electrically Erasable PROMs (EEPROMs), EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture

RAM Fault Modeling

Electrical Testing, Peusdo Random Testing, Megabit DRAM Testing, Non-volatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing

General Reliability Issues

RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Reliability Modeling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, RAM Fault Modeling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Non-volatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing

Radiation Effects

Single Event Phenomenon (SEP), Radiation Hardening Techniques-Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test Structures, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto-resistive Random Access Memories (MRAMs), Experimental Memory Devices, Memory Hybrids and MCMs (2D) Memory Stacks and MCMs (3D) Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging Future Directions

Text Books :

1. Ashok K. Sharma, *Semiconductor Memories*, Two-Volume Set, Wiley-IEEE Press, 2003

2. Brent Keeth, R. Jacob Baker, *DRAM Circuit Design A Tutorial*, Wiley-IEEE Press, 2000

Reference Books :
1. Betty Prince, *High Performance Memories New Architecture DRAMs and SRAMs - Evolution and Function*, Wiley, 1999
Question Paper Pattern:
Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions **End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

PRINCIPLES OF DISTRIBUTED EMBEDDED SYSTEMS (PDES)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC959 (Elective-IV)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand C language and assembly programming.

CO2: Understand Object orientation for programming and C++.

CO3: Understand software modeling fundamentals.

CO4: Understand Embedded software development tools

REAL-TIME ENVIRONMENT

Real-time computer system requirements – classification of real time systems – simplicity – global time – internal and external clock synchronization – real time model. Real – time communication – temporal relations – dependability – power and energy awareness – real –time communication – event triggered – rate constrained – time triggered

UNIT II - REAL-TIME OPERATING SYSTEMS

Inter component communication – task management – dual role of time – inter task interactions – process input/output – agreement protocols – error detection

SYSTEM DESIGN

Scheduling problem - static & dynamic scheduling – system design – validation – time–triggered architecture

INTRODUCTION TO CAN

Introduction to CAN Open – CAN open standard – Object directory – Electronic Data Sheets & Devices

CAN STANDARDS

Configuration Files – Service Data Objectives – Network management CAN open messages – Device Profile Encoder

Text Books :

1.Hermann Kopetz, “Real–Time systems – Design Principles for distributed Embedded Applications”, 2nd Edition, Springer 2011.

2. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Copperhill Media Corporation, 2008.

Reference Books :

1.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

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EMBEDDED LINUX (ELX)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC960 (Elective-IV)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand fundamentals of Embedded Linux.

CO2: Understand GNU tool chain.

CO3: Understand Embedded Linux applications

CO4: Understand Embedded Development Environment

Linux Fundamentals

Introduction - host-target development setup - hardware support - development languages and tools – RT linux.

Initialization

Linux kernel and kernel initialization - system initialization – hardware support – boot loaders.

Device Handling

Device driver basics - module utilities - file systems - MTD subsystems – busy box.

Development Tools

Embedded development environment - GNU debugger - tracing & profiling tools - binary utilities - kernel debugging - debugging embedded Linux applications - porting Linux - Linux and real time - SDRAM interface.

Device Applications

Asynchronous serial communication interface - parallel port interfacing - USB interfacing - memory I/O interfacing - using interrupts for timing.

Text Books :

2. *Embedded Linux Primer: A practical real world approach*, Christopher Hallinan, Prentice Hall, 2007.

2. *Embedded Linux: Hardware, software and Interfacing*, Craig Hollabaugh, Pearson Education, 2002.

Reference Books :

4. *Building embedded linux systems*, Karim Yaghmour, Jon Masters, Gillad Ben Yossef, Philippe Gerum, O'Reilly, 2008.

5. *Linux for embedded and real time applications*, Doug Abbott, Elsevier Science, 2003.

Question Paper Pattern:

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EMBEDDED NETWORKS AND PROTOCOLS (ENP)

II Semester : VLSI & ES					Scheme : 2017		
Course Code	Hours/Week			Credits	Maximum Marks		
EC961 (Elective-IV)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand concepts of CAN protocals and ethernet.

CO2: Understand elements of a network.

CO3: Understand industrial networking protocals.

CO4: Understand RF communication

INTRODUCTION TO CAN

The CAN bus - General - Concepts of bus access and arbitration - Error processing and management - From concept to reality -Patents, licenses and certification – CAN protocol: 'ISO 11898-1'- Content of the different ISO/OSI layers of the CAN bus-Compatibility of CAN 2.0A and CAN 2.0B

ETHERNET BASICS

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

EMBEDDED ETHERNET

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

INDUSTRIAL NETWORKING PROTOCOL

LIN – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus - Audiovideo buses - I2C Bus - D2B (Domestic digital) bus - MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'- profi bus.

RF COMMUNICATION

Radio-frequency communication: internal and external - Remote control of opening parts - PKE (passive keyless entry) and passive go- TPMS (tyre pressure monitoring systems) -Wireless networks GSM-Bluetooth - IEEE 802.11x - NFC (near-field communication).

Text Books :

1. *Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire*, Dominique Paret, John Wiley & Sons Ltd- 2007.
2. *Embedded Ethernet and Internet Complete,* Jan Axelson Penram publications

Reference Books :

1. *Embedded networking with CAN and CAN open,*. Glaf P.Feiffer, Andrew Ayre and Christian Keyold Embedded System Academy 2005
2. *Principles of Embedded Networked Systems Design*, Gregory J. Pottie, William J. Kaiser Cambridge University Press, Second Edition, 2005.

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End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

HARDWARE SOFTWARE CO-DESIGN (HSC)

II Semester : VLSI & ES					**Scheme : 2017**		
Course Code	**Hours/Week**			**Credits**	**Maximum Marks**		
EC962 (Elective-IV)	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
	3	**-**	**-**	**3**	**40**	**60**	**100**
Sessional Exam Duration : 2 Hrs					**End Exam Duration: 3 Hrs**		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand H/W and S/W Co Design models.

CO2: Understand H/W and S/W prototyping and target architectures

CO3: Understand H/W and S/W design specifications and verification

CO4: Understand the H/W and S/W system level synthesis

Co- Design Issues

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Prototyping and Emulation

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions. **Target Architectures:** Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

Languages for System – Level Specification and Design-I,II

System – level specification, design representation for system level synthesis, system level specification languages. Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books :

2. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Reference Books :

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

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End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions