M.Tech Syllabus- Scheme 2017
(VLSI and Embedded Systems)
<table>
<thead>
<tr>
<th>S. No.</th>
<th>Course No.</th>
<th>Course Title</th>
<th>Credits</th>
<th>Scheme of Instruction periods/week</th>
<th>Scheme of Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>1</td>
<td>EC851</td>
<td>CMOS Analog IC Design (AICD)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>EC852</td>
<td>Advanced Digital System Design using Verilog (ADSD)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>EC853</td>
<td>Embedded Real Time Operating System (ERTOS)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>EC854</td>
<td>Advanced Embedded systems (AES)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>Elective – I</td>
<td></td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>Elective–II</td>
<td></td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>AU101</td>
<td>Technical English</td>
<td>-</td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>EC863</td>
<td>Advanced VLSI and Embedded Systems Lab (AVESP)</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td><strong>20</strong></td>
<td><strong>20</strong></td>
<td><strong>3</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Course No.</th>
<th>Course Title</th>
<th>Credits</th>
<th>Scheme of Instruction periods/week</th>
<th>Scheme of Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>1</td>
<td>EC951</td>
<td>Low Power VLSI Design (LVD)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>EC952</td>
<td>VLSI Design for Testability (VDFT)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>EC953</td>
<td>VLSI Architecture (VLSIA)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>EC954</td>
<td>Microcontrollers for Embedded System Design (MESD)</td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>Elective – III</td>
<td></td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>Elective – IV</td>
<td></td>
<td>3</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>AU102</td>
<td>Research Methodology (RM)</td>
<td>-</td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>EC963</td>
<td>Advanced Electronic Design Automation Lab (EDAP)</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td><strong>20</strong></td>
<td><strong>20</strong></td>
<td><strong>3</strong></td>
</tr>
</tbody>
</table>
# List of Subjects for Electives

<table>
<thead>
<tr>
<th>Description</th>
<th>Subject title</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elective-I</td>
<td>CMOS Digital IC Design (DICD)</td>
<td>EC855</td>
</tr>
<tr>
<td></td>
<td>CPLD and FPGA ARCHITECTURES and APPLICATIONS (FPGA)</td>
<td>EC856</td>
</tr>
<tr>
<td></td>
<td>Scripting Languages for VLSI Design Automation (SLA)</td>
<td>EC857</td>
</tr>
<tr>
<td></td>
<td>VLSI Technology (VTECH)</td>
<td>EC858</td>
</tr>
<tr>
<td>Elective II</td>
<td>Embedded Programming (EP)</td>
<td>EC859</td>
</tr>
<tr>
<td></td>
<td>Embedded System Architecture (ESA)</td>
<td>EC860</td>
</tr>
<tr>
<td></td>
<td>Robotics and Automation (RAA)</td>
<td>EC861</td>
</tr>
<tr>
<td></td>
<td>Advanced Computer Networks (ACN)</td>
<td>EC862</td>
</tr>
<tr>
<td>Elective III</td>
<td>VLSI Signal Processing (VS)</td>
<td>EC955</td>
</tr>
<tr>
<td></td>
<td>Electronic Design Automation Tools (EDAT)</td>
<td>EC956</td>
</tr>
<tr>
<td></td>
<td>System on Chip Architecture (SOCA)</td>
<td>EC957</td>
</tr>
<tr>
<td></td>
<td>Design of Semiconductor Memories(DSM)</td>
<td>EC958</td>
</tr>
<tr>
<td>Elective IV</td>
<td>Principles of Distributed Embedded Systems (PDES)</td>
<td>EC959</td>
</tr>
<tr>
<td></td>
<td>Embedded Linux (ELX)</td>
<td>EC960</td>
</tr>
<tr>
<td></td>
<td>Embedded Networks and Protocols (ENP)</td>
<td>EC961</td>
</tr>
<tr>
<td></td>
<td>Hardware Software Co-design (HSC)</td>
<td>EC962</td>
</tr>
</tbody>
</table>
### Course Outcomes

At the end of the course the student will be able to

- **CO1**: design simple and high impedance current mirror circuits and their frequency response
- **CO2**: design Differential OP-AMP and comparator circuits
- **CO3**: design Sample and hold and switched capacitor circuits
- **CO4**: understand Nyquist rate Data converters
- **CO5**: understand Oversampling Data converters and filters

### Basic current mirrors and single stage amplifiers

- Simple CMOS current mirror, common source, Common gate amplifier with current mirror active load, Source follower with current mirror to supply bias current, High output impedance current mirrors and bipolar gain stages, Frequency response.

### Operational amplifier design and compensation

- Two stage CMOS operational amplifier, feedback and operational amplifier compensation, advanced current mirrors, Folded-cascode operational amplifier, Current mirror operational amplifier, Fully differential operational amplifier, common mode feedback circuits, Current feedback operational amplifier. Comparator, Charge injection error, Latched comparators, BiCMOS comparators.

### Sample and hold and switched capacitor circuits

- MOS, CMOS and BiCMOS sample and hold circuits, Switched capacitor circuits, Basic operation and analysis, first order and biquad filters, Charge injection, Switched capacitor gain circuit, Correlated double sampling techniques, Other switched capacitor circuits.

### Data converters


### Over sampling converters and filters

- Over sampling with and without noise shaping, Digital decimation filter, High order modulators, Band pass over sampling converters, Practical Considerations, Continuous time filters, first order and second order filters, introduction to $G_{in-c}$ filters.

### Text Books


### Reference Books

**Web References:**

1. http://nptel.ac.in/courses/117106030/35
2. https://link.springer.com/chapter/10

**Question Paper Pattern:**

**Internal Assessment:** The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

**End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions
I Semester : VLSI & ES
Course Code: EC852

<table>
<thead>
<tr>
<th>Course Outcomes:</th>
<th>At the end of the course the student will be able to</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1:</td>
<td>Analyze and design sequential digital circuits</td>
</tr>
<tr>
<td>CO2:</td>
<td>Analyze and design asynchronous sequential digital</td>
</tr>
<tr>
<td></td>
<td>circuits</td>
</tr>
<tr>
<td>CO3:</td>
<td>Design using programmable logic devices</td>
</tr>
<tr>
<td>CO4:</td>
<td>Identify the requirements and specifications of the</td>
</tr>
<tr>
<td></td>
<td>system required for a given application</td>
</tr>
<tr>
<td>CO5:</td>
<td>Design and use programming tools for implementing</td>
</tr>
<tr>
<td></td>
<td>digital circuits of industry standards</td>
</tr>
</tbody>
</table>

SEQUENTIAL CIRCUIT DESIGN
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

SYSTEM DESIGN USING VERILOG

Text Books:

Reference Books:

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
EMBEDDED REAL TIME OPERATING SYSTEM (ERTOS)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC853</td>
<td>L T P C</td>
<td>Continuous Internal Assessment</td>
<td>End Exam</td>
</tr>
<tr>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
<td>100</td>
</tr>
</tbody>
</table>

Sessional Exam Duration : 2 Hrs  End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to

CO1: Understand Real Time Systems and RTOS functionality
CO2: Understand the UNIX file system and its Programming
CO3: Understand the VxWorks, Posix, μC/OS-II and RT Linux environments
CO4: Understand the debugging tools for suitable RTOS Environments

Concept of Embedded Operating Systems

Interprocess Communication (IPC):

UNIX Operating Systems

RTOS Environments
POSIX Real Time Extensions, Software Logic Analyzers, ICEs. Comparison of RTOS, VxWorks, μC/OS-II and RT Linux for Embedded Applications.

Debugging Tools
OTP emulators, On board emulation of Software using Cross Development Environments, Software Logic Analyzers, ICEs.

Text Books:

Reference Books:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
ADVANCED EMBEDDED SYSTEMS (AES)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC854</td>
<td>L T P C</td>
<td>Continuous Internal Assessment</td>
<td>End Exam</td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

Sessional Exam Duration: 2 Hrs
End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to

CO1: Understand Intel 8051 and Atmel microcontrollers features for embedded systems
CO2: Utilize the programming model of 8051 microcontroller in framing various programs.
CO3: Understand the Embedded C programming techniques for microcontrollers.
CO4: Use Embedded C in interfacing of I/O peripherals to microcontrollers

Introduction to embedded systems
Background and History of Embedded Systems, Definition and Classification, Programming languages for embedded systems. Processor and Memory Organization: Structural units in processor, Processor selection for an embedded system, Memory devices, Memory selection, Allocation for memory to program segments and blocks and memory map of a system.

8051 Microcontroller and operations

Programming Structure
Programs using 8051 instruction set. Introduction to embedded C, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version). Example: Reading switch inputs (basic code), Example: Counting goats

Adding Structure to the Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the ‘Hello Embedded World’ example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

Meeting Real-Time Constraints
Introduction, Creating ‘hardware delays’ using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2. The need for ‘timeout’ mechanisms, Creating loop timeouts. Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout.

Text Books:

Reference Books:

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
## TECHNICAL ENGLISH (TE)

### I Semester: Common for All M.Tech Programmes

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Category</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>AU101</td>
<td>Audit Course</td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td>-</td>
</tr>
</tbody>
</table>

**Sessional Exam Duration:** -  |  **End Exam Duration:** -

### Course Outcomes:

At the end of the course students will be able to

**CO 1:** write Technical Reports, Journal Papers and Project Reports.

**CO 2:** write Job Applications, Resumes and Statements of Purpose.

### Course Content

1. Technical Reports – Formats and Styles
   - a) Feasibility Report
   - b) Factual Report
   - c) Project Reports
2. Journal Papers – Formats
3. Paper Presentation Strategies
4. Statement of Purpose for Internships and Apprenticeships
5. Letter Writing – Job Applications, Resume Preparation
6. Common Errors in Research Papers

### Reference Books:

### Course Details

**Course Code:** EC863

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC863</td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>3</td>
</tr>
</tbody>
</table>

**End Exam Duration:** 3 Hrs

**Course Outcomes:** At the end of the course the student will be able to

- **CO1:** Understand HDL programming models.
- **CO2:** Design various digital circuits using CPLD and FPGA devices.
- **CO3:** Synthesize various Digital circuits.
- **CO4:** Program MSP 430 and Cortex M4 Processors

### List of Experiments

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
7. Microcontroller programming using MSP430 and Cortex M4 processors
   - a) Toggling the LEDs,
   - b) Master Slave Communication,
   - c) PWM interface
   - d) Sensor Interfacing (Temperature)

**Internal Assessment:** 50M

**End Exam:** 50M
LOW POWER VLSI DESIGN (LVD)

<table>
<thead>
<tr>
<th>II Semester : VLSI &amp; ES</th>
<th>Scheme : 2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Course Code</td>
<td>Hours/Week</td>
</tr>
<tr>
<td>EC951</td>
<td>L  T  P C</td>
</tr>
<tr>
<td></td>
<td>3  -  -</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Sessional Exam Duration</strong> : 2 Hrs</td>
<td><strong>End Exam Duration</strong> : 3 Hrs</td>
</tr>
</tbody>
</table>

**Course Outcomes**

At the end of the course the student will be able to

**CO1:** Understand different sources of power dissipation

**CO2:** Understand minimization of switched capacitance

**CO3:** Analyze and minimize dynamic and static power consumption in VLSI circuits

**CO4:** Understand working principles of adiabatic logic

**CO5:** Find ways to minimize power in software design

**Sources of Power Dissipation**

Short-Circuit Power Dissipation, Switching Power Dissipation, Glitching Power Dissipation, Leakage Power Dissipation; Power Sources- for low power circuits---chargeable and disposable batteries, **Supply Voltage Scaling for Low Power:** Device Feature Size Scaling, Architectural-Level Approaches, Voltage Scaling Using High-Level Transformations, Multilevel Voltage Scaling, Challenges in MVS, Dynamic Voltage and Frequency Scaling, Adaptive Voltage Scaling, Subthreshold Logic Circuits

**Switched Capacitance Minimization**


**Leakage Power Minimization**


**Adiabatic Logic Circuits**

Adiabatic Charging, Adiabatic Amplification, Adiabatic Logic Gates, Pulsed Power Supply, Stepwise Charging Circuits

**Low-Power Software Approaches**

Introduction, Machine-Independent Software Optimizations, Combining Loop Optimizations with DVFS: Loop Unrolling, Loop Tiling, Loop Permutation, Strength Reduction, Loop Fusion, Loop Peeling, Loop Un switching

**Text Books :**


**Reference Books :**

**Web References:**

1. nptel.ac.in/courses/106105034/

**Question Paper Pattern:**

**Internal Assessment:** The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

**End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions
VLSI DESIGN FOR TESTABILITY (VDFT)

<table>
<thead>
<tr>
<th>II Semester : VLSI &amp; ES</th>
<th>Scheme : 2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Course Code</td>
<td>Hours/Week</td>
</tr>
<tr>
<td>EC952</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

**Sessional Exam Duration : 2 Hrs**  
**End Exam Duration: 3 Hrs**

**Course Outcomes :** At the end of the course the student will be able to

- CO1: Understand all the levels of testing done in VLSI circuits
- CO2: Understand the DFT principles in VLSI circuits
- CO3: Understand logic and fault simulation in VLSI circuits
- CO4: Generate test generation in VLSI circuits

**Introduction to Testing**
Importance of Testing, Testing During the VLSI Lifecycle, Challenges in VLSI Testing- Challenges in VLSI Testing, Fault Models; Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology

**Design for Testability**
Introduction, Testability Analysis——SCOAP Testability Analysis, Probability-Based Testability Analysis, Simulation-Based Testability Analysis; Design for Testability Basics—— Ad Hoc Approach, Structured Approach; Scan Cell Designs--Muxed-D Scan Cell, Clocked-Scan Cell, LSSD Scan Cell; Scan Architectures --- Full-Scan Design, Partial-Scan Design, Random-Access Scan Design; Scan Design Rules, Scan Design Flow diagram and brief description of each stages only, RTL Design for Testability

**Logic and Fault Simulation**

**Test Generation**
Introduction, Random Test Generation, Boolean difference, untestable faults, Designing a Stuck-At ATPG for Combinational Circuits--- A Naive ATPG Algorithm, A Basic ATPG Algorithm, D Algorithm, PODEM, PODEM; Designing a Sequential ATPG--- Designing a Sequential ATPG, 5-Valued Algebra Is Insufficient, Gated Clocks and Multiple Clocks; Untestable Fault Identification, ATPG for Non-Stuck-At Faults--- Designing an ATPG That Captures Delay Defects, ATPG for Transition Faults.

**Logic Built-In Self-Test**

**Text Books :**

**Reference Books :**

**Web References:**
2. [https://onlinecourses.nptel.ac.in/noc17_ec02/preview](https://onlinecourses.nptel.ac.in/noc17_ec02/preview)
3. [http://nptel.ac.in/courses/106103116/](http://nptel.ac.in/courses/106103116/)

**Question Paper Pattern:**

**Internal Assessment:** The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

**End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions
II Semester : VLSI & ES

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC953</td>
<td>L T P C</td>
<td>Continuous Internal Assessment</td>
<td>End Exam</td>
</tr>
<tr>
<td>3 - 40 60 100</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sessional Exam Duration: 2 Hrs
End Exam Duration: 3 Hrs

Course Outcomes:

CO1: Students will be in position to choose processor architecture for their projects.
CO2: Students will be able to work with DSP processors and understand MAC architecture.
CO3: Students will be able learn advanced concepts in super scalar architectures.

Complex Instruction Set Computers (CISC)
Instruction Set, Characteristics and Functions, Addressing Modes, Instruction Formats, Architectural Overview, Processor Organization, Register Organization, Instruction Cycle, Instruction Pipelining, Pentium Processor, PowerPC Processor

Reduced Instruction Set Computers (RISC)
Instruction execution Characteristics, Register Organization, Reduced Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview, RISC Pipelining, Motorola 88510, MIPS R4650, RISC Vs. CISC

DSP Processors
Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview

Pipeline Processing
Basic Concepts, Classification of Pipeline Processors, Instruction and Arithmetic Pipelining, Design of Pipelined Instruction Units, Pipelining Hazards and Scheduling, Principles of Designing Pipelined Processors

Super Scaler Processors
Overview, Design Issues, PowerPC, Pentium

Text Books:

Reference Books:

Question Paper Pattern:

Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
# MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN (MESD)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC954</td>
<td>L T P C</td>
<td>Continuous Internal Assessment</td>
<td>End Exam</td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

| Sessional Exam Duration : 2 Hrs | End Exam Duration: 3 Hrs |

## Course Outcomes:
At the end of the course the student will be able to

- **CO1:** Understand ARM Architecture and pipelining.
- **CO2:** Understand ARM processor instruction set and thumb formats
- **CO3:** Use ARM programming model to frame programs
- **CO4:** Understand the memory management and cache issues of ARM processor

### ARM Architecture
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

### ARM Programming Model – I
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

### ARM Programming Model – II
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

### ARM Programming
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

### Memory Management

### Text Books:

### Reference Books:

### Question Paper Pattern:
- **Internal Assessment:** The question paper shall consist of Six questions out of which the student shall answer any Four questions
- **End Exam:** The question paper shall consist of Eight questions out of which the student shall answer any Five questions
## RESEARCH METHODOLOGY (RM)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Continuous Internal Assessment</th>
<th>End Exam</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>AU102</td>
<td>L</td>
<td>T</td>
<td>P</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Course Outcomes:

- **CO1:** Understand overview of research process, state the research problem and conduct a literature review of the concepts comprising the research questions.
- **CO2:** Study the data collection methods and process the data statistically.
- **CO3:** Understand the basic properties of estimators, analyse the estimated data and interpret the data in a research paper.

### Meaning, Objective and Motivation in Research


### Measurement and Scaling Techniques


### Methods of Data Collection

Primary Data, Questionnaire and Interviews, Collection of Secondary Data, Cases and Schedules.

### Statistical Processing

Correlation and Regression Analysis, Method of Least Squares, Regression Vs. Correlation, Correlation Vs. Determination, Types of Correlation and Their Specific Applications.

### Hypothesis Testing


### Interpretation of Data

Data interpretation, Layout of a Research Paper, Techniques of Interpretation.

### Text Books / Reference Books:

ADVANCED ELECTRONIC DESIGN AUTOMATION LAB (AEDAP)

<table>
<thead>
<tr>
<th>II Semester : VLSI &amp; ES</th>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EC963</td>
<td>L  T  P</td>
<td>C</td>
<td>Continuous Internal Assessment</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-  -  3</td>
<td>2</td>
<td>50</td>
</tr>
</tbody>
</table>

End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to

CO1: Perform transient, AC and DC analysis of CMOS based circuits

CO2: Perform transient, AC and DC analysis of PASS-transistor based circuits

CO3: Perform transient, AC and DC analysis of Transmission Gate based circuits

CO4: Perform transient, AC and DC analysis of circuits like CS, CG, CD, Diff Amplifier, Op-Amp etc.

CO5: Perform DRS, LVS, Layouts of simple circuits.

LIST OF EXPERIMENTS

1. Transient Analysis of various CMOS based circuits (from simple circuits like Inverter to complex circuits like arithmetic circuits).

2. Transient Analysis of PASS Transistor based circuits

3. Transient Analysis of various Transmission Gate (TG) based circuits (e.g. XOR gate, MUX etc).

4. Transient, AC, DC Analysis of various amplifier circuits (e.g. CS, CD, Differential, Operational Amplifiers etc.). Finding CMRR (for Differential and Operational Amplifiers) and Bandwidth.

5. Applications based on operational amplifiers (e.g. DAC etc.)

6. DRC, LVS, Parasitic Values Estimation from Layout of CMOS based circuits.

Reference Books:


Internal Assessment: 50M

End Exam: 50M
I Semester: VLSI & ES

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC855</td>
<td>L T P</td>
<td>C</td>
<td>Continuous Internal Assessment</td>
</tr>
<tr>
<td>(Elective-I)</td>
<td>3 3  -</td>
<td>3</td>
<td>40</td>
</tr>
</tbody>
</table>

Sessional Exam Duration: 2 Hrs

End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to

CO1: Revise the MOS transistor theory
CO2: Solve various delays in combinational circuit and its optimization methods
CO3: Understand circuit design of latches and flip-flops.
CO4: Understand combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
CO5: Understand Design Methodology and Tools

MOS Transistor Theory Review
Introduction, Long-Channel I-V Characteristics, C-V Characteristics: Simple MOS Capacitance Models, Detailed MOS Gate Capacitance Model; Non-ideal I-V Effects: Mobility Degradation and Velocity Saturation, Channel Length Modulation, Threshold Voltage Effects, Leakage, Temperature Dependence; DC Transfer Characteristics

Combinational network delay
Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis

Sequencing static circuits

Data path and array subsystems
Addition / Subtraction. Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Design Methodology and Tools
Introduction, Structured Design Strategies using with the help of Software Radio Example, Design Methods, Design Flows

Text Books:

Reference Books:

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions

Page 19 of
### CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (FPGA)

**I Semester : VLSI & ES**

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Continuous Internal Assessment</th>
<th>End Exam</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC856 (Elective-I)</td>
<td>L</td>
<td>T</td>
<td>P</td>
<td>C</td>
<td>End Exam</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

**Course Outcomes:** At the end of the course the student will be able to

- **CO1:** Understand ROMs, PALs, PLAs, CPLDs
- **CO2:** Get exposure to industry standard FPGAs of XILINX, ALTERA and ACTEL in terms of programming technology, logic block implementation, interconnect structures, and their I/Os.
- **CO3:** Understand the concepts of ASICs and its design Flow
- **CO4:** Understand System partitioning, floor-planning Placement & Routing and associated algorithms

### CPLD

Programmable logic, Programmable read only memory (PROM), programmable logic array (PLA), Programmable array logic (PAL). Sequential programmable logic devices (SPLDS), Programmable gate arrays (PGAS), CPLD

### FPGA Programming Technology

Programmable logic FPGA general structure, Anti fuse - Static RAM: EPROM and EEPROM technology, PREP benchmarks, FPGA Logic block – Actel ACT - Xilinx LCA, Altera FLEX, Altera MAX;

### FPGA I/Os

DC & AC inputs and outputs, Clock and Power inputs, Xilinx I/O block

### FPGA Interconnect

Actel ACT -Xilinx LCA - Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX 9000, Altera FLEX, FPGA Design flow

### ASIC Construction

Physical Design ,Goals and objectives of all the ASIC physical design steps, System partitioning, Partitioning method—Constructive partitioning, iterative partitioning, K-L algorithm, Floor planning ,Floor planning tools ,Placement , placement Methods, Placement types-- constructive: min-cut placement method, eigenvalue placement algorithm, Iterative Placement Improvement, Physical design flow.

### ASIC Routing

Global Routing : Goals and Objectives , Measurement of Interconnect Delay ,Global routing Methods, Detailed routing: Goals and objectives, Measurement of channel density, Left Edge Algorithm, Circuit Extraction and DRC, Special Routing : Clock Routing and Power Routing .

### Text Books :


### Reference Books :

**Web References:**

3. www.asic.co.in/

**Question Paper Pattern:**

**Internal Assessment:** The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions.

**End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions.
SCRIPTING LANGUAGES FOR VLSI DESIGN AUTOMATION (SLA)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC857</td>
<td>L T P C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Elective-I)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

Sessional Exam Duration: 2 Hrs
End Exam Duration: 3 Hrs

Course Outcomes:

CO1: Students are capable of scripting the given code in HDLs.
CO2: Students will get benefit of using Scripting languages in their projects.
CO3: Students will get scope for learning Java Script, SKILL etc.

Overview of scripting languages:

PERL, File handles, Operators, Control structures, Regular expressions, Built in data types, Operators, Statements and declarations- simple, Compound, Loop statements, Global and scoped declarations.

Pattern matching:

Regular expression, Pattern matching operators, Character classes, Positions, capturing and clustering.

Subroutines:

Syntax, Semantics, Proto types, Format variables, References, Data structures, Arrays of arrays, Hashes of arrays, Hashes of functions, Inter process communication, Signals, Files, Pipes, sockets.

Threads:

Process model, Thread model, Perl debugger, Using debugger commands, Customization, Internals and externals, Internal data types, Extending perl, embedding perl, Exercises for programming using perl.

Other languages:

Broad features of other scripting languages SKILL, CGI, java script, VB script

Text Books / Reference Books:


Question Paper Pattern:

Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions

End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
# VLSI TECHNOLOGY (VTECH)

## Course Code: EC858 (Elective-I)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Continuous Assessment</th>
<th>End Exam</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC858</td>
<td>L T P C</td>
<td></td>
<td></td>
<td>End Exam</td>
<td>TOTAL</td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>End Exam</td>
<td>60</td>
<td>100</td>
</tr>
</tbody>
</table>

**Sessional Exam Duration:** 2 Hrs  
**End Exam Duration:** 3 Hrs

## Course Outcomes:

- **CO1:** Understand the MOS technologies, its models and latch-up problem
- **CO2:** Understand the layout design and layouts of logic gates
- **CO3:** Understand all the stages of manufacturing an IC
- **CO4:** Understand the doping and deposition concepts
- **CO5:** Understand design rules and scaling, BICMOS ICs in

## Review of Microelectronics and Introduction to MOS Technologies

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & BiCMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

## Layout Design


## Stages of Manufacturing

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

## Doping and Depositions

Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitaxy, molecular beam epitaxy

## Design rules and Scaling, BICMOS ICs

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

## Text Books:


## Reference Books:

2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
EMBEDDED PROGRAMMING (EP)

I Semester : VLSI & ES    Scheme : 2017

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC859</td>
<td>L T P C</td>
<td>Continuous Internal Assessment</td>
<td>End Exam</td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

Sessional Exam Duration : 2 Hrs   End Exam Duration: 3 Hrs

Course Outcomes : At the end of the course the student will be able to

CO1: Understand C language and assembly programming.
CO2: Understand Object orientation for programming and C++.
CO3: Understand software modeling fundamentals.
CO4: Understand Embedded software development tools

INTRODUCTION TO ASSEMBLY LANGUAGE AND DATAREPRESENTATION IN C


PROGRAMMING IN C


OBJECT ORIENTED PROGRAMMING

Object oriented analysis and design - C++ classes and objects – functions – data structures - examples

UNIFIED MODELING LANGUAGE


EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS

The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS

Text Books :

Reference Books :

Question Paper Pattern:

Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
EMBEDDED SYSTEM ARCHITECTURE (ESA)

Course Code | Hours/Week | Credits | Continuous Internal Assessment | End Exam | TOTAL
---|---|---|---|---|---
EC860 (Elective-II) | L | T | P | C | |
| 3 | 0 | - | 3 | 40 | 60 | 100

Sessional Exam Duration : 2 Hrs

End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to
- **CO1**: Understand the Embedded System Models
- **CO2**: Understand the typical engineering issues of software development.
- **CO3**: Understand rationale and concepts for designing embedded systems
- **CO4**: Analyze the Embedded Issues of Software

### Introduction to embedded systems


### Processor Hardware


### Support Hardware


### Software


### Engineering Issues Of Software

Design and development: architectural patterns and reference models – creating the architectural structures – documenting the architecture – analyzing and evaluating the architecture – debugging testing, and maintaining.

**Text Books**:  

**Reference Books**:  

**Question Paper Pattern:**

**Internal Assessment**: The question paper shall consist of Six questions out of which the student shall answer any Four questions

**End Exam**: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
## Course Outcomes
At the end of the course the student will be able to

**CO1:** Understand anatomy and laws of robotics

**CO2:** Understand the micro machines and types of the control modes.

**CO3:** Understand the forward kinematics and its techniques.

**CO4:** Use robot programming tools in robot cell design

### Basic Concepts
Definition and origin of robotics – different types of robotics – various generations of robots – degrees of freedom – Asimov’s laws of robotics – anatomy of robot - applications of robots.

### Power Sources And Sensors

### Manipulators, Actuators And Grippers
Construction of manipulators – manipulator dynamics and force control – types of control modes- electronic and pneumatic manipulator control circuits – end effectors – various types of grippers.

### Kinematics And Path Planning
Forward kinematics-solution of inverse kinematics problem – multiple solution jacobian work envelop – hill climbing techniques – robot programming languages

### Case Studies

### Text Books


### Reference Books


### Question Paper Pattern:
**Internal Assessment:** The question paper shall consist of Six questions out of which the student shall answer any **Four** questions

**End Exam:** The question paper shall consist of Eight questions out of which the student shall answer any **Five** questions
ADVANCED COMPUTER NETWORKS (ACN)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Continuous Internal Assessment</th>
<th>End Exam</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC862 (Elective-II)</td>
<td>L</td>
<td>T</td>
<td>P</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>0</td>
<td>-</td>
<td>3</td>
<td>40</td>
</tr>
</tbody>
</table>

Sessional Exam Duration : 2 Hrs
End Exam Duration: 3 Hrs

Course Outcomes:

CO1: Understand Intel 8051 and Atmel microcontrollers features for embedded systems

CO2: Utilize the programming model of 8051 microcontroller in framing various programs.

CO3: Understand the Embedded C programming techniques for microcontrollers.

CO4: Use Embedded C in interfacing of I/O peripherals to microcontrollers

Congestion and Quality of Service (QoS)


Wireless Local Area Networks


Cellular Systems and Infrastructure


ATM Protocol Reference Model


Interconnection Networks


Text Books:

<table>
<thead>
<tr>
<th>Reference Books</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Introduction to Broadband Communication Systems- Sadiku, Mathew N.O., Akujuobi, Cajetan.M, PHI</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Question Paper Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Internal Assessment</strong>: The question paper shall consist of <strong>Six</strong> questions out of which the student shall answer any <strong>Four</strong> questions</td>
</tr>
<tr>
<td><strong>End Exam</strong>: The question paper shall consist of <strong>Eight</strong> questions out of which the student shall answer any <strong>Five</strong> questions</td>
</tr>
</tbody>
</table>
Course Outcomes: At the end of the course the student will be able to

CO1: Apply the principles of DFG in DSP architectures.

CO2: Apply pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.

CO3: Solve Register minimization, retiming, folding techniques for the given digital filter.

CO4: Understand the overview FIR filter Systolic architecture design.

Introduction to Digital Signal Processing Systems

Introduction, Typical DSP Algorithms, DSP Application demands and scaled CMOS technologies, Representation of DSP Algorithms.

Iteration Bound


 Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power.

Retiming and Unfolding

Introduction, Definitions and properties, Solving systems of inequalities, Retiming Techniques, An algorithm for unfolding, Critical path, Unfolding and retiming, Applications of unfolding.

Folding

Introduction, Folding techniques, Register minimization techniques, Register minimization in folded architecture, Folding of multirate systems.

Systolic Architecture Design

Introduction, System array design methodology, FIR systolic arrays, selection of scheduling vector, Matrix-matrix multiplication and 2-D systolic array design, Systolic Design for space representations containing delays.

Text Books:


Reference Books:


Question Paper Pattern:

Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions

End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
II Semester: VLSI & ES  
Course Code: EC956 (Elective-III)  

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L T P C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EC956</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

Course Outcomes:
At the end of the course the student will be able to:

- **CO1**: Utilize EDA tools in their projects.
- **CO2**: Design synthesizable verilog code.
- **CO3**: Explain the difference between verilog and systemverilog and write SystemVerilog code.
- **CO4**: Design circuits using Pspice.

Synthesis and simulation using HDLs

Circuit commands for simulation using Spice
- Circuit description AC, DC and transient analysis, Advanced spice commands and analysis-SUBCKT, ENDS, FUNC, GLOBAL, INC, LIB, NODESET, options, PARAM, Fourier analysis, Noise Analysis, SENS, STEP, DC.

Circuit simulation using Spice
- Models for diodes, transistors and opamp. Digital logic circuits-digital gates and timing models, flip flops and latches.

Data Types in SystemVerilog
- Introduction, data types-Built-In Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Array Methods, Choosing a Storage Type, typedef, User-Defined Structures, Packages, Type Conversion, Streaming Operators, Enumerated Types, Constants, Strings.

Design of Procedures, routines and basic test benches in SystemVerilog

Text Books:
2. M.H.Rashid, Spice for Circuits and Electronics using Pspice. (2/e), PHI.

Reference Books:

Question Paper Pattern:
**Internal Assessment**: The question paper shall consist of Six questions out of which the student shall answer any Four questions.

**End Exam**: The question paper shall consist of Eight questions out of which the student shall answer any Five questions.
SYSTEM ON CHIP ARCHITECTURE (SOCA)

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC957</td>
<td>L T P C</td>
<td>Continuous Internal Assessment</td>
<td>End Exam</td>
</tr>
<tr>
<td></td>
<td>3 - - 3</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

Sessional Exam Duration: 2 Hrs  End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to

- **CO1:** understand system approach for SoC design
- **CO2:** understand processor design as part of SoC design
- **CO3:** understand Memory design as part of SoC design
- **CO4:** understand interconnect optimization and configuration in an SoC
- **CO5:** understand applications of SoC with the help of case studies

Introduction to the System Approach


Processors

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors

Memory Design for SOC


Interconnect Customization and Configuration


Application Studies / Case Studies

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books:


Reference Books:

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM

Question Paper Pattern:

**Internal Assessment:** The question paper shall consist of Six questions out of which the student shall answer any Four questions

**End Exam:** The question paper shall consist of Eight questions out of which the student shall answer any Five questions
DESIGN OF SEMICONDUCTOR MEMORIES (DSM)

II Semester : VLSI & ES

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC958 (Elective-III)</td>
<td>L T P C Continuous Internal Assessment End Exam TOTAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 - - 3 40 60 100</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sessional Exam Duration : 2 Hrs
End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to
CO1: Students will get insight into basic memory techniques to advanced memory techniques.
CO2: Students will be able to analyze faults in memories.
CO3: Students will be able to use efficient memory techniques in their projects especially testing phase.

SRAM Cell Structures
MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies, Silicon On Insulator (SOI) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs

DRAM Technology Development
CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS, DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

Masked Read-Only Memories (ROMs)
High Density ROMs, Programmable Read-Only Memories (PROMs)-Bipolar PROMs, CMOS PROMs-Erasable (UV), Programmable Read-Only Memories (EPROMs), Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs, Electrically Erasable PROMs (EEPROMs), EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture

RAM Fault Modeling

General Reliability Issues

Radiation Effects
Single Event Phenomenon (SEP), Radiation Hardening Techniques-Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test Structures, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto-resistive Random Access Memories (MRAMs), Experimental Memory Devices, Memory Hybrids and MCMs (2D) Memory Stacks and MCMs (3D) Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging Future Directions

Text Books:
**Reference Books :**


**Question Paper Pattern:**

**Internal Assessment:** The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

**End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions
Course Code: EC959

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Hours/Week</th>
<th>Credits</th>
<th>Maximum Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC959</td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td>(Elective-IV)</td>
<td>3</td>
<td>-</td>
<td>3</td>
</tr>
</tbody>
</table>

Sessional Exam Duration : 2 Hrs

Course Outcomes: At the end of the course the student will be able to

CO1: Understand C language and assembly programming.
CO2: Understand Object orientation for programming and C++.
CO3: Understand software modeling fundamentals.
CO4: Understand Embedded software development tools

REAL-TIME ENVIRONMENT

UNIT II - REAL-TIME OPERATING SYSTEMS
Inter component communication – task management – dual role of time – inter task interactions – process input/output – agreement protocols – error detection

SYSTEM DESIGN
Scheduling problem - static & dynamic scheduling – system design – validation – time–triggered architecture

INTRODUCTION TO CAN
Introduction to CAN Open – CAN open standard – Object directory – Electronic Data Sheets & Devices

CAN STANDARDS
Configuration Files – Service Data Objectives – Network management CAN open messages – Device Profile Encoder

Text Books:

Reference Books:
1.

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
EMBEDDED LINUX (ELX)

II Semester : VLSI & ES  
Course Code  | Hours/Week | Credits | Maximum Marks
--- | --- | --- | ---
EC960 (Elective-IV)  |  |  |  
| L | T | P | C | Continuous Internal Assessment | End Exam | TOTAL
| 3 | - | - | 3 | 40 | 60 | 100

Sessional Exam Duration : 2 Hrs  
End Exam Duration: 3 Hrs

Course Outcomes: At the end of the course the student will be able to
CO1: Understand fundamentals of Embedded Linux.
CO2: Understand GNU tool chain.
CO3: Understand Embedded Linux applications
CO4: Understand Embedded Development Environment

Linux Fundamentals
Introduction - host-target development setup - hardware support - development languages and tools – RT linux.

Initialization
Linux kernel and kernel initialization - system initialization – hardware support – boot loaders.

Device Handling
Device driver basics - module utilities - file systems - MTD subsystems – busy box.

Development Tools

Device Applications
Asynchronous serial communication interface - parallel port interfacing - USB interfacing - memory I/O interfacing - using interrupts for timing.

Text Books :

Reference Books :

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
End Exam: The question paper shall consist of Eight questions out of which the student shall answer any Five questions
EMBEDDED NETWORKS AND PROTOCOLS (ENP)

II Semester : VLSI & ES  
Course Code  |  Hours/Week  |  Credits  |  Maximum Marks  
--- | --- | --- | ---
EC961 (Elective-IV)  |  L  |  T  |  P  |  C  |  Continuous Internal Assessment  |  End Exam  |  TOTAL  
3  |  -  |  -  |  3  |  40  |  60  |  100  

Sessional Exam Duration : 2 Hrs  
End Exam Duration: 3 Hrs  

Course Outcomes: At the end of the course the student will be able to

CO1: Understand concepts of CAN protocols and ethernet.

CO2: Understand elements of a network.

CO3: Understand industrial networking protocols.

CO4: Understand RF communication

INTRODUCTION TO CAN
The CAN bus - General - Concepts of bus access and arbitration - Error processing and management - From concept to reality - Patents, licenses and certification – CAN protocol: ‘ISO 11898-1’ - Content of the different ISO/OSI layers of the CAN bus-Compatibility of CAN 2.0A and CAN 2.0B

ETHERNET BASICS

EMBEDDED ETHERNET

INDUSTRIAL NETWORKING PROTOCOL

RF COMMUNICATION
Radio-frequency communication: internal and external - Remote control of opening parts - PKE (passive keyless entry) and passive go- TPMS (tyre pressure monitoring systems) -Wireless networks GSM-Bluetooth - IEEE 802.11x - NFC (near-field communication).

Text Books:
2. *Embedded Ethernet and Internet Complete*, Jan Axelsson Penram publications

Reference Books:

Question Paper Pattern:
Internal Assessment: The question paper shall consist of Six questions out of which the student shall answer any Four questions
**HARDWARE SOFTWARE CO-DESIGN (HSC)**

<table>
<thead>
<tr>
<th>II Semester : VLSI &amp; ES</th>
<th>Scheme : 2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Course Code</td>
<td>Hours/Week</td>
</tr>
<tr>
<td>EC962 (Elective-IV)</td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
</tr>
</tbody>
</table>

**Sessional Exam Duration : 2 Hrs**  
**End Exam Duration: 3 Hrs**

**Course Outcomes**: At the end of the course the student will be able to

- **CO1**: Understand H/W and S/W Co Design models.
- **CO2**: Understand H/W and S/W prototyping and target architectures
- **CO3**: Understand H/W and S/W design specifications and verification
- **CO4**: Understand the H/W and S/W system level synthesis

**Co-Design Issues**

Co-Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co-Synthesis Algorithms**: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

**Prototyping and Emulation**

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions. **Target Architectures**: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

**Compilation Techniques and Tools for Embedded Processor Architectures**

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment

**Design Specification and Verification**

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

**Languages for System – Level Specification and Design-I,II**

System – level specification, design representation for system level synthesis, system level specification languages. Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

**Text Books**:


**Reference Books**:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

**Question Paper Pattern**:

**Internal Assessment**: The question paper shall consist of Six questions out of which the student shall answer any Four questions
**End Exam:** The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions.