G. PULLA REDDY ENGINEERING COLLEGE (Autonomous): KURNOOL

Accredited by NBA of AICTE and NAAC of UGC

An ISO 9001:2008 Certified Institution

Affiliated to JNTUA, Anantapuramu

Two-Year M. Tech Degree Program

M.Tech Scheme & Syllabus - Scheme 2022

(VLSI and Embedded Systems)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
TWO YEAR M. TECH DEGREE PROGRAM
Scheme of Instruction and Examination
(Effective from 2022-2023)

I Semester – VLSI and Embedded Systems (VLSI & ES) **Scheme – 2022**

S. No.	Category	Course Title	L	T	P	Credits	End Exam Marks	CIA Marks	Total
I		**Theory**							
1.	PC	Digital VLSI Design	3	-	-	3	60	40	100
2.	PC	Advanced Embedded Systems	3	-	-	3	60	40	100
3.	PC	Advanced Digital System Design Using Verilog	3	-	-	3	60	40	100
4.	PE	Professional Elective – I	3	-	-	3	60	40	100
5.	PE	Professional Elective – II	3	-	-	3	60	40	100
6.	MC	Research Methodology & IPR	2	-	-	2	-	100	100
7.	AC	Audit Course - I	2	-	-	0	-	-	-
II		**Practical**							
8.	PCL	Advanced VLSI Lab	-	-	3	2	60	40	100
9.	PCL	Advanced Embedded Systems Lab	-	-	3	2	60	40	100
			19	**-**	**6**	**21**	**420**	**380**	**800**

II Semester – VLSI and Embedded Systems (VLSI & ES) **Scheme – 2022**

S. No.	Category	Course Title	L	T	P	Credits	End Exam Marks	CIA Marks	Total
I		**Theory**							
1.	PC	Analog IC Design	3	-	-	3	60	40	100
2.	PC	Embedded Systems for Internet of Things	3	-	-	3	60	40	100
3.	PE	Professional Elective – III	3	-	-	3	60	40	100
4.	PE	Professional Elective – IV	3	-	-	3	60	40	100
5.	PE	Professional Elective – V	3	-	-	3	60	40	100
6.	AC	Audit Course - II	2	-	-	0	-	-	-
II		**Practical**							
7.	PCL	Advanced Electronic Design Automation Lab	-	-	3	2	60	40	100
8.	PCL	Embedded IoT Lab	-	-	3	2	60	40	100
			17	**-**	**6**	**19**	**420**	**280**	**700**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
TWO YEAR M. TECH DEGREE PROGRAM
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III Semester – VLSI and Embedded Systems (VLSI & ES) **Scheme – 2022**

S. No.	Category	Course Title	L	T	P	Credits	End Exam Marks	CIA Marks	Total
1.	OE	Open Elective (OE) *	2	-	-	2	-	-	100
2.	PR	Dissertation Phase – I	-	-	20	10	-	100	100
3.	CAA	Co – Academic Activities	-	-	-	2	-	100	100
	Total		**2**	**-**	**20**	**14**	**-**	**200**	**300**

*Open Elective will be offered through MOOCs

IV Semester – VLSI and Embedded Systems (VLSI & ES) **Scheme – 2022**

S. No.	Category	Course Title	L	T	P	Credits	End Exam Marks	CIA Marks	Total
1	PR	Dissertation Phase - II	-	-	**32**	**16**	**60**	**40**	**100**

List of Professional Elective Courses

Description	Subject Title
PE – I	Hardware Algorithms for Computer Arithmetic(HACA)
	Scripting Languages for VLSI Design Automation (SLVA)
	VLSI Technology (VTECH)
PE – II	Embedded Programming (EP)
	Embedded System Architecture (ESA)
	Hardware Software Co-design (HSC)
PE – III	Physical Design Automation(PDA)
	CAD for VLSI Design(CVD)
	Mixed Signal Circuit Design(MSCD)
PE – IV	Embedded Networks and Protocols (ENP)
	Microcontrollers for Embedded System Design(MESD)
	Principles of Distributed Embedded Systems (PDES)
PE – V	VLSI Design For Testability(VDFT)
	Memory Design and Testing(MDT)
	VLSI Signal Processing (VS)

Open Elective

OE	Open Elective will be selected through MOOCs

List of Audit Courses

Description	Subject Title
Audit Course – I	Disaster Management
	English for research Paper Writing
	Sanskrit for Technical Knowledge
Audit Course – II	Pedagogy Studies
	Personality Development through Life Enlightenment Skills
	Stress Management by Yoga

I Semester – VLSI and Embedded Systems (VLSI & ES) **Scheme – 2022**

S. No.	Category	Course Title	L	T	P	Credits	End Exam Marks	CIA Marks	Total
I		**Theory**							
1.	PC	Digital VLSI Design	3	-	-	3	60	40	100
2.	PC	Advanced Embedded Systems	3	-	-	3	60	40	100
3.	PC	Advanced Digital System Design Using Verilog	3	-	-	3	60	40	100
4.	PE	Professional Elective – I	3	-	-	3	60	40	100
5.	PE	Professional Elective – II	3	-	-	3	60	40	100
6.	MC	Research Methodology & IPR	2	-	-	2	-	100	100
7.	AC	Audit Course - I	2	-	-	0	-	-	-
II		**Practical**							
8.	PCL	Advanced VLSI Lab	-	-	3	2	60	40	100
9.	PCL	Advanced Embedded Systems Lab	-	-	3	2	60	40	100
			19	**-**	**6**	**21**	**420**	**380**	**800**

DIGITAL VLSI DESIGN (DVD)

I Semester :VLSI & ES				Scheme : 2022			
Course Code	Hours/Week			Credits	Maximum Marks		
EC 851	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Analyze the MOSFET based circuits and their synthesis

CO2:Draw the layout/stick diagram of CMOS logic circuits.

CO3:Analyze the performance of CMOS logic circuits

CO4: Design CMOS combinational and dynamic logic circuits.

INTRODUCTION

Basic MOSFET Characteristics – Threshold Voltage, Body Bias concept, Current- Voltage Characteristics – Square-Law Model, MOSFET Modeling – Drain-Source Resistance, MOSFET Capacitances, Geometric Scaling Theory – Full-Voltage Scaling, Constant-Voltage Scaling, Challenges of MOSFET Scaling.

LAYOUT OF CMOS LOGIC CIRCUITS &SWITCHING PROPERTIES

CMOS fabrication processing steps, Design Rules, Stick diagram, Layout of logic circuits, latch-up.Static and dynamic characteristics of Pass Transistors, Transmission Gate, TG based logic circuits.

CMOS INVERTER & STATIC CMOS LOGIC ELEMENTS

Basic Circuit and DC Operation – DC Characteristics, Noise Margins, Layout considerations, Inverter Switching Characteristics, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance, Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads.CMOS NAND Gate, CMOS NOR Gate, Complex Logic Functions, CMOS SRAM Cell.

POWER DISSIPATION IN CMOS DIGITAL CIRCUITS

Dynamic Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power Dissipation – Diode Leakage Current, Subthreshold Leakage Current.

DYNAMIC LOGIC CIRCUIT CONCEPTS AND CMOS DYNAMIC LOGIC FAMILIES

Charge Leakage, charge Sharing, Dynamic RAM Cell, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Single-Phase Logic.Issues in Chip Design:ESD Protection, On-Chip Interconnects – Line Parasitics, Modeling of the Interconnect Line, Clock Distribution, Input-Output circuits.

Text Books :

1.Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGrawHill (2008) 3rd

2. J P Uyemura, CMOS Circuit Design, Springer

Reference Books :

1.Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, Edition Wesley (1998) 2nd ed.

2. Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.

3.Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.

4..Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design perspective, Pearson Education (2007) 2nd ed.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of**Six**questions out of which the student shall answer any **Four** questions.

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ADVANCED EMBEDDED SYSTEMS (AES)

I Semester :VLSI & ES				Scheme : 2022			
Course Code	Hours/Week			Credits	Maximum Marks		
EC 852	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand features, characteristics and applications of embedded systems

CO2: Understand the categories of microcontrollers and their operations.

CO3: Analyze the architecture of MSP430 family processors

CO4: Utilize the programming model of MSP430 for interfacing applications

CO5: Create application interfaces using the programming tools of advanced microcontrollers

Introduction to embedded systems

Background and History of Embedded Systems, Definition and Classification, Programming languages for embedded systems. **Processor and Memory Organization:** Structural units in processor, Processor selection for an embedded system, Memory devices, Memory selection, Allocation for memory to program segments and blocks and memory map of a system.

Microcontroller and operations

Microprocessors Vs Microcontrollers, 8051 Family, Architecture, Pin Functions, Addressing Modes, Instruction Set. The external interface of the Standard 8051, Memory issues, I/O pins, Timers, Interrupts, Serial interface.

Architecture of the MSP430 Processor:

Central Processing Unit, Addressing Modes, ConstantGenerator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and InstructionSet, Resets, Clock System, Memory and memory Organization.

Digital Input, Output, and Displays:

Parallel Ports, Digital Inputs, Switch Debounce, Digital Outputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.

MSP430 Case Studies

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I2C.

Text Books :

1. Raj Kamal, Embedded Systems Architecture, Programming and Design,2nd Edition, TMH, 2006.

2.John H. Davies,MSP430 Microcontroller Basics, Elsevier Ltd Publications, Copyright 2008.

Reference Books :

1.Frank Vahid, Tony D. Givargis, “Embedded system Design: A Unified Hardware/Software Introduction”, John Wily & Sons Inc.2002.

Web Reference

https://onlinecourses.nptel.ac.in/noc12cs11/course

Question Paper Pattern:

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End Exam: The question paper shall consist of**Eight**questions out of which the student shall answerany **Five** questions

ADVANCED DIGITAL SYSTEM DESIGN USING VERILOG (ADSD)

I Semester :VLSI & ES				Scheme : 2022			
Course Code	Hours/Week			Credits	Maximum Marks		
EC 852	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Analyze and design sequential digital circuits

CO2: Analyze and design asynchronous sequential digital circuits

CO3: Design using programmable logic devices

CO4: Identify the requirements and specifications of the system required for a given application

CO5: Design and use programming tools for implementing digital circuits of industry standards

SEQUENTIAL CIRCUIT DESIGN

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

SYSTEM DESIGN USING VERILOG

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

Text Books :

2. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
3. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001

Reference Books :

1. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
2. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
3. M.D.Ciletti ,Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.
4. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

Question Paper Pattern:

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End Exam: The question paper shall consist of**Eight**questions out of which the student shall answerany **Five** questions

ADVANCED VLSI LAB

I Semester : VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 860	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	-	-	3	2	40	60	100

End Exam Duration: 3 Hrs

Course Outcomes : At the end of the course the student will be able to

CO1: Analyze HDL programming models.

CO2: Design various digital circuits using FPGA devices

CO3: Synthesize various Digital circuits.

CO4: Design Placement & Routing Techniques

LIST OF EXPERIMENTS

1. Digital Circuits Description using Verilog
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Combinational Digital circuits
5. Synthesis of Sequential Digital circuits
6. Place and Route techniques for major FPGA vendor such as Xilinx
7. Implementation of Designed Digital Circuits using FPGA devices
8. Digital Circuits Description using VHDL/Verilog

Internal Assessment:40M

End Exam: 60M

ADVANCED EMBEDDED SYSTEMSLAB (AES(P))

ISemester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 861	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	0	0	3	2	40	60	100
End Exam Duration: 3 Hrs							
Course Outcomes : At the end of the course the student will be able to							
CO1: Interpret the level of programs done in Code Composer Studio IDE							
CO2: Interface the I/O peripherals with MSP430 controller.							
CO3:Interface the sensors and actuators with MSP430 controller.							
CO4:Interface co processing devices with MSP430 controller							
List of Experiments							
1. Utilization and Practice of Code Composer Studio 2. Interfacing on board output elements with MSP430 controller 3. Interfacing on board input and output elements with MSP430 controller 4. Interfacing Arrays of Lights with MSP430 controller 5. Interfacing Motor applications with MSP430 controller 6. Interfacing onboard sensor with MSP430 controller 7. Interfacing external sensor with MSP430 controller 8. Interfacing displays with MSP430 controller 9. Interfacing multiple sensors with MSP430 controller 10. Interfacing a sub controller under supervisor control with MSP430 controller							
Internal Assessment: 40M End Exam:60M							

Hardware Algorithms for Computer Arithmetic (HACA)

I Semester :VLSI & ES				Scheme : 2022			
Course Code	Hours/Week			Credits	Maximum Marks		
EC 854 (Professional Elective – I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1:Understand the Redundant number systems

CO2:Analyze Algorithms for fast addition

CO3:Analyze VLSI implementation aspects, High speed multiplication

CO4: Interpret Algorithms for fast division and impact of hardware technology

Algorithms for Fast Addition

Basic Addition and Counting, Bit-serial and ripple-carry adders, Addition of a constant: counters, Manchester carry chains and adders, Carry-Look-ahead Adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in Fast Adders, Simple carry-skip and Carry-select adders, Hybrid adder designs, Optimizations in fast adders, Multi-Operand Addition, Wallace and Dadda trees, Parallel counters, Generalized parallel counters, Adding multiple signed numbers.

High-Speed Multiplication

Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers, VLSI layout considerations.

Fast Division and Division Through Multiplication

Basic Division Schemes, Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Division by Convergence, Hardware implementation.

Digital Input, Output, and Displays:

Square-Rooting Methods, The CORDIC Algorithms, Computing algorithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by Table Lookup, Tradeoffs in cost, speed, and accuracy.

Function Evaluation

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I2C.

Text Books :

1 .Parhami, B., Computer Arithmetic: Algorithms and Hardware Design, Oxford University Press (2000).

2. Ercegovac, M. and Lang, T., Digital Arithmetic, Elsevier (2005).

Reference Books :

1 .Koren, I., Computer Arithmetic Algorithms, 2nd Edition, Uni Press (2005) 2nd ed.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

SCRIPTING LANGUAGES FOR VLSI DESING AUTOMATION (SLVA)

I Semester : VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 855 (Professional Elective – I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: scripting the given code in HDLs

CO2: Utilize Scripting languages in their projects.

CO3: AnalyzeJava Script, SKILL etc.

Overview of scripting languages

PERL, File handles, Operators, Control structures, Regular expressions, Built in data types, Operators, Statements and declarations- simple, Compound, Loop statements, Global and scoped declarations

Pattern matching

expression, Pattern matching operators, Character classes, Positions, capturing and clustering.

Subroutines

Syntax, Semantics, Proto types, Format variables, References, Data structures, Arrays of arrays, Hashesof arrays, Hashes of functions, Inter process communication, Signals, Files, Pipes, sockets.

Threads

Process model, Thread model, Perl debugger, Using debugger commands, Customization, Internals and externals, Internal data types, Extending perl, embedding perl, Exercises for programming using perl.

Other languages

Broad features of other scripting languages SKILL, CGI, java script, VB script

Text Books / Reference Books :

1. Larry Wall, Tom Christiansen, John Orwant, *Programming perl*, 3rd Edition, Oreilly publications
2. Randal L, Schwartz Tom Phoenix, *Learning PERL*, Oreilly publications

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of**Eight**questions out of which the student shall answerany **Five** questions

VLSI TECHNOLOGY (VTECH)

I Semester :VLSI & ES				Scheme : 2022			
Course Code	Hours/Week			Credits	Maximum Marks		
EC 856 (Professional Elective – I)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand the MOS technologies, its models and latch-up problem

CO2: Design the layouts of logic gates

CO3: Interpret the stages of manufacturing an IC

CO4: Analyze the doping and deposition procedures

CO5: Analyze design rules and scaling, BICMOS ICs

Review of Microelectronics and Introduction to MOS Technologies

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

Layout Design

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

Stages of Manufacturing

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

Doping and depositions

Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy

Design rules and Scaling, BICMOS ICs

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations.

Text Books :

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997

2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

Reference Books :

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning 2011

2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

EMBEDDED PROGRAMMING(EP)

I Semester :VLSI & ES				Scheme : 2022			
Course Code	**Hours/Week**			**Credits**	**Maximum Marks**		
EC 857 (Professional Elective – II))	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
	3	**-**	**-**	**3**	**40**	**60**	**100**
Sessional Exam Duration : 2 Hrs				**End Exam Duration: 3 Hrs**			

Course Outcomes : At the end of the course the student will be able to

CO1: Analyze C language and assembly programming.

CO2: Utilize Object orientation for programming and C++.

CO3: Apply software modelling fundamentals.

CO4: Analyze Embedded software development tools

INTRODUCTION TO ASSEMBLY LANGUAGE AND DATAREPRESENTATION IN C

Assembly language programming – macros - Data representation – Twos complement, fixed point and floating point number formats –Low level programming in C: Primitive data types – Pointers – Structures – Unions – Dynamic memory allocation – Functions – recursive functions - Linked lists.

PROGRAMMING IN C

Register usage conventions – Typical use of addressing options – Instruction sequencing – Procedure call and return – Functions – recursive functions – 8, Parameter passing – Retrieving parameters – Everything in pass by value – Temporary variables – threads – pre-emptive kernels – system timer – scheduling

OBJECT ORIENTED PROGRAMMING

Object oriented analysis and design - C++ classes and objects – functions – data structures – examples

UNIFIED MODELING LANGUAGE

Connecting the object model with the use case model – Key strategies for object identification – UML basics. Object state behavior – UML state charts – Role of scenarios in the definition of behaviour – Timing diagrams – Sequence diagrams – Event hierarchies – types and strategies of operations – Architectural design in UML concurrency design – threads in UML

EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS

The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS

Text Books :

1. David E. Simon, " *An Embedded Software Primer*", Pearson Education, 2003

2. Daniel W. Lewis, " *Fundamentals of embedded software where C and assembly meet*", Pearson Education, 2002.

Reference Books :

1. Steve Heath, " *Embedded system design*", Elsevier, 2003.

2. E. Balaguruswamy, " *Object oriented programming with C++*", Tata McGraw Hill, 2011.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

EMBEDDED SYSTEMS ARCHITECTUTRE (ESA)

I Semester : VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 858 (Professional Elective – II)	L	T	P	C	Continuous Internal Assessment	End Exam	Total
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand the Embedded System Models
CO2: Analyze the typical engineering issues of software development.
CO3: Interpret rationale and concepts for designing embedded systems
CO4: Analyze the Embedded Issues of Software

Introduction to embedded systems

Embedded system model – embedded standards – block diagrams – powering the hardware - embedded board using Von Neuman model. Embedded processors: ISA architecture models – application specific ISA models – general purpose ISA models – instruction level parallelism.

Processor Hardware

Internal processor design: ALU – registers – control unit - clock – on chip memory – processor i/o – interrupts – processor buses – processor performance.

Support Hardware

Board memory: ROM – RAM – cache – auxiliary memory – memory management memory performance – board buses: arbitration and timing – PCI bus example integrating bus with components – bus performance

Software

Middleware and applications: PPP – IP middleware – UDP – Java .application layer: FTP client SMTP – HTTP server and client

Engineering Issues Of Software

Design and development: architectural patterns and reference models – creating the architectural structures – documenting the architecture – analyzing and evaluating the architecture – debugging testing, and maintaining.

Text Books :

1. *Embedded system architecture*, Tammy Noergaard, Elsevier, 2006.

Reference Books :

1. *Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C*, Jean J.Labrosse, The publisher, Paul Temme, 2011.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

HARDWARE SOFTWARE CO-DESIGN (HSC)

I Semester : VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 859 (Professional Elective – II)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand H/W and S/W Co Design models.

CO2: Understand H/W and S/W prototyping and target architectures

CO3: Analyze H/W and S/W design specifications and verification

CO4: Analyze the H/W and S/W system level synthesis

Co- Design Issues

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware–software partitioning distributed system co-synthesis

Prototyping and Emulation

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions. **Target Architectures:** Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

Languages for System – Level Specification and Design-I,II

System – level specification, design representation for system level synthesis, system level specification languages. Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books :

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Reference Books :

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

Question Paper Pattern

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

RESEARCH METHODOLOGY& IPR(RM& IPR)

I Semester : VLSI & ES				Scheme : 2022			
Course Code	Hours/Week			Credits	Maximum Marks		
MC 101	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	2	100	-	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: - 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1: Understand overview of research process, state the research problem and conduct a literature review of the concepts comprising the research questions.

CO2: Study the data collection methods and process the data statistically.

CO3: Understand the basic properties of estimators, analyse the estimated data and interpret the data in a research paper.

Meaning, Objective and Motivation in Research

Types of Research, Research Approaches, Research Process, Validity and Reliability in Research. Features of Good Design, Types of Research Design, Basic Principles of Experimental Design, Steps in Sampling Design, Characteristics of a Good Sample Design, Random Samples and Random Sampling Design.

Measurement and Scaling Techniques

Errors in Measurement, Tests of Sound Measurement, Scaling and Scale Construction Techniques, Forecasting Techniques, Time Series Analysis, Interpolation and Extrapolation.

Methods of Data Collection

Primary Data, Questionnaire and Interviews, Collection of Secondary Data, Cases and Schedules.

Statistical Processing

Correlation and Regression Analysis, Method of Least Squares, Regression Vs. Correlation, Correlation Vs. Determination, Types of Correlation and Their Specific Applications.

Hypothesis Testing

Tests of Hypothesis, Parametric Vs. Non-Parametric Tests, Procedure for Testing Hypothesis, Use of Statistical Techniques for Testing Hypothesis, Sampling Distribution, Sampling Theory Chi-Square Test, Analysis of Variance and Covariance, Multivariable Analysis

Interpretation of Data

Data interpretation, Layout of a Research Paper, Techniques of Interpretation.

Text Books / Reference Books :

1. C.R. Kothari, *Research Methodology (Methods & Techniques)*, New Age International Publishers.
2. R.Cauvery, V.K.SudhaNayak, M.Girija, Research Methodology, S.Chand Publishers.

List of Audit Courses

Description	Subject Title
Audit Course – I	Disaster Management
	English for research Paper Writing
	Sanskrit for Technical Knowledge

DISASTER MANAGEMENT
(Audit Course – I for M. Tech-I Semester)

I Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
AU 101	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	0	-	-	-

Course Outcomes : At the end of the course the student will be able to

CO1: Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO2: Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO3: Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO4: Critically understand the strengths and weaknesses of disaster management approaches,

CO5: Planning and programming in different countries, particularly their home country or the countries they work in

UNIT - I

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT - II

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters:Earthquakes,Volcanisms,Cyclones,Tsunamis,Floods,DroughtsandFamines,LandslidesandAvalanches, Man-made disaster:Nuclear Reactor Meltdown,Industrial Accidents,Oil Slicks andSpills,OutbreaksofDisease and Epidemics,WarandConflicts.

UNIT - III

Disaster Preparedness and Management: Preparedness:MonitoringofPhenomenaTriggering a DisasterorHazard;EvaluationofRisk:ApplicationofRemoteSensing,Data fromMeteorologicalandOtherAgencies,MediaReports:Governmentaland CommunityPreparedness.

UNIT – IV

Risk Assessment Disaster Risk:
ConceptandElements,DisasterRiskReduction,GlobalandNationalDisasterRiskSituation.Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People'sParticipationin RiskAssessment.StrategiesforSurvival.

UNIT – V

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation inIndia.

Text Books :

1. R.Nishith,SinghAK,"DisasterManagementinIndia:Perspectives,issuesandstrategies"'NewRoyalbookCompany.

Reference Books :

1. Sahni,PardeepEt.Al.(Eds.),"DisasterMitigationExperiencesandReflections",PrenticeHallofIndia, NewDelhi.
2. GoelS.L.,Disaster Administration and Management Text and CaseStudies",Deep&DeepPublicationPvt. Ltd., Delhi.

ENGLISH FOR RESEARCH PAPERWRITING
(Audit Course – I for M. Tech-I Semester)

I Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
AU 101	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	0	-	-	-

Course Outcomes : At the end of the course the student will be able to

CO1: Understand that how to improve your writing skills and level of readability

CO2: Learn about what to write in each section

CO3: Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT - I

Overview of a Research Paper – Planning and Preparation – Word Order – Useful Phrases – Breaking up Long Sentences – Structuring Paragraphs and Sentences – Being Concise and Removing Redundancy – Avoiding Ambiguity

UNIT - II

Essential Components of a Research Paper – Abstracts – Building Hypothesis – Research Problem – Highlight Findings – Hedging and Criticizing – Paraphrasing and Plagiarism – Cauterization.

UNIT - III

Introducing Review of the Literature – Methodology – Analysis of the Data – Findings – Discussion – Conclusions – Recommendations

UNIT - IV

Key skills needed when writing a Title – Abstract – Introduction.

UNIT - V

Appropriate language to formulate Methodology – Incorporate Results – Put forth Arguments and draw Conclusions

Text Books :

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

Reference Books :

1. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

SANSKRIT FOR TECHNICAL KNOWLEDGE

(Audit Course – I for M. Tech-I Semester)

I Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
AU 101	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	0	-	-	-

Course Outcomes : At the end of the course the student will be able to

CO1: Understanding basic Sanskrit language

CO2: Ancient Sanskrit literature about science & technology can be understood

CO3: Being a logical language will help to develop logic in students

UNIT - I

Alphabets in Sanskrit,

UNIT - II

Past/Present/Future Tense, Simple Sentences

UNIT - III

Order, Introduction of roots

UNIT - IV

Technical information about Sanskrit Literature

UNIT - V

Technical conceptsofEngineering-Electrical,Mechanical,Architecture,Mathematics

Text Books :

1. "Abhyaspustakam"–Dr.Vishwas, Samskrita-BhartiPublication,NewDelhi

Reference Books :

1. "TeachYourselfSanskrit"PrathamaDeeksha-VempatiKutumbshastri,RashtriyaSanskritSansthanam,NewDelhi Publication
2. "India'sGloriousScientificTradition"Suresh Soni, Ocean Books(P)Ltd.,NewDelhi.

II Semester – VLSI and Embedded Systems (VLSI & ES) **Scheme – 2022**

S. No.	Category	Course Title	L	T	P	Credits	End Exam Marks	CIA Marks	Total
I		**Theory**							
1.	PC	Analog IC Design	3	-	-	3	60	40	100
2.	PC	Embedded Systems for Internet of Things	3	-	-	3	60	40	100
3.	PE	Professional Elective – III	3	-	-	3	60	40	100
4.	PE	Professional Elective – IV	3	-	-	3	60	40	100
5.	PE	Professional Elective – V	3	-	-	3	60	40	100
6.	AC	Audit Course - II	2	-	-	0	-	-	-
II		**Practical**							
7.	PCL	Advanced Electronic Design Automation Lab	-	-	3	2	60	40	100
8.	PCL	Embedded IoT Lab	-	-	3	2	60	40	100
			17	**-**	**6**	**19**	**420**	**280**	**700**

ANALOG IC DESIGN (AICD)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 951	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs				End Exam Duration: 3 Hrs			

Course Outcomes : At the end of the course the student will be able to

CO1:Acquire a basic knowledge of analog IC design including small signal models, analog MOS processes and layout techniques.

CO2: Analyze the frequency responses of single stage amplifiers.

CO3: Analyze and design two-stage operational amplifier.

CO4: Design of single stage and differential stage amplifiers with and without current mirror circuits, respectively.

Basic MOSFET Physics

IV Characteristics, Second order effects, MOS Device Models and Small Signal MOS Transistor Models.

Analog MOS Process

Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors, Passive devices: Capacitors and Resistors, Substrate Coupling, Ground Bounce.

Amplifiers and Current sources

Large Signal and Small-Signal analysis of common source stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode, differential amplifier, current Sources, Basic Current Mirrors, Cascode Current Mirrors and current mirror based differential amplifier.

Frequency Response of Amplifiers & Voltage References

Dynamic Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power Dissipation – Diode Leakage Current, Subthreshold Leakage Current.

Operational Amplifier

General Considerations, Theory and Design, Performance Parameters, Design of 2-stage MOS Operational Amplifier, Gain Boosting, slew rate, Offset effects, PSRR, Stability and Frequency Compensation, topologies, familiarity with non linearity and mismatch.

Text Books :

1.Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (2008).

2. Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.

Reference Books :

1. Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002) 2nd ed.

2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (2004).

. Hastings, A., The Art of Analog Layout, Prentice Hall (2005).

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions.
End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions.

EMBEDDED SYSTEMS IN INTERNET OF THINGS(EIoT)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 952	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand the basic knowledge of Internet of things and its design

CO2: Interpretthe purpose of sensors and Actuators in IoT

CO3: Analyze Various IoT Protocols

CO4: Design IoT Projects Using Arduino

CO5: Analyze Raspberry-Pi Processor and Raspbian Operating Systems

Introduction to IoT:

Definition and Characteristics of IoT, Physical Design and Logical Design, IoT Enabling Technologies, IoT Levels and Deployment Templates, IoT Vs M2M

Sensors and Actuators

Definition of Sensor, Sensor features, Resolution, Classes, Different types of sensors, Actuator, Different types of Actuators, purpose of Sensors and Actuators in IoT

Building IoT with Arduino

Arduino IDE, Programming of Arduino, Interfacing LED, switch, potentiometer, Sensors, LCD, Bluetooth, Wi-Fi, ,GPS, RFID with Arduino

Wireless Technologies and Data Transmission for IoT

Wi-Max, Wi-Fi (802.11), Bluetooth/Bluetooth smart,Zigbee/Zigbee smart, Cellular, NFC,Serial Transmission, RS-232, RS-485, I2C Inter-Integrated Circuit, Ethernet, CAN bus, USB, Firewall, Serial ATA, Parallel Transmission

Raspberry Pi

Raspberry Pi Processor, Raspberry Pi Vs Arduino, Operating system benefits, Raspberry Pi Set up, Configuration

Text Books :

1. ArsheepBahga , Vijay Madisetti ,Internet of Things: A Hands-On Approach Paperback,2015
2. RajkumarBhuyya ,Internet of Things : Principles and Paradigms,2016

Reference Books :

1.CharlesBell,Beginning Sensor Networks with Arduino and Raspberry-Pi,Apress,2016.

2.Warren Gay,Masteringthe Raspberry-Pi,Apress,2016

Web Reference

https://onlinecourses.nptel.ac.in/noc17_cs22/course

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

ADVANCED ELECTRONIC DESIGNAUTOMATION LAB (EDAP)

II Semester :VLSI & ES						**Scheme : 2022**	
Course Code	**Hours/Week**			**Credits**	**Maximum Marks**		
EC 962	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
	-	**-**	**3**	**2**	**40**	**60**	**100**

END EXAM DURATION : 3 Hrs

Course Outcomes : At the end of the course the student will be able to

CO1: Perform Transient, AC and DC analysis of CMOS based circuits

CO2:.Perform Transient, AC and DC analysis of PASS-transistor based circuits

CO3: Perform Transient, AC and DC analysis of Transmission Gate based circuits

CO4: Perform Transient, AC and DC analysis of circuits like CS,CG,CD, Diff Amplifier, Op-Amp etc.

CO5: Perform DRS,LVS, Layouts of simple circuits.

LIST OF EXPERIMENTS

1. Transient Analysis of various CMOS based circuits (from simple circuits like Inverter to complex circuits like arithmetic circuits).
2. Transient Analysis of PASS Transistor based circuits
3. Transient Analysis of various Transmission Gate (TG) based circuits (eg. XOR gate, MUX etc).
4. Transient, AC, DC Analysis of various amplifier circuits (e.g. CS, CD, Differential, Operational Amplifiers etc.). Finding CMRR (for Differential and Operational Amplifiers) and Bandwidth.
5. Applications based on operational amplifiers (e.g. DAC etc.)
6. DRC, LVS, Parasitic Values Estimation from Layout of CMOS based circuits.

Internal Assessment: 40M

End Exam: 60M

EMBEDDED IoT LAB (EIoT(P))

II Semester :VLSI & ES						Scheme : 2022
Course Code	Hours/Week			Credits	Maximum Marks	
EC 963	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	-	-	3	2	40	60	100

END EXAM DURATION : 3 Hrs

Course Outcomes : At the end of the course the student will be able to

CO1: Interpret the level of programs done in Arduino IDE and Embedded C

CO2:. Interface the I/O peripherals with ATmega controller.

CO3: Interface the sensors and actuators with ATmega controller.

CO4: Perform Interface Internet applications with Arduino and Rasp pi processors

LIST OF EXPERIMENTS

1. Utilization and Practice of Rasp Pi Environment and Arduino Environment
2. Interfacing on board output elements with ATmega controller
3. Interfacing on board input and output elements with ATmega controller
4. Interfacing laser light with ATmega controller
5. Interfacing chemical sensor with ATmega controller
6. Interfacing temperature sensor with ATmega controller
7. Interfacing touch based sensor with ATmega controller
8. Interfacing displays with MSP430 controller
9. Interfacing multiple sensors with MSP430 controller
10. Interfacing an I/O board controlled by using Raspberry Pi controller

Internal Assessment: 40M

End Exam: 60M

PHYSICAL DESIGN AUTOMATION (PDA)

II Semester :VLSI & ES					**Scheme : 2022**		
Course Code	**Hours/Week**			**Credits**	**Maximum Marks**		
EC 953 (Professional Elective – III)	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
	3	**-**	**-**	**3**	**40**	**60**	**100**
Sessional Exam Duration : 2 Hrs					**End Exam Duration: 3 Hrs**		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand of VLSI Design Automation.

CO2: Acquire knowledge about CAD tools used for VLSI design.

CO3: Analyze Algorithms for VLSI Design Automation.

CO4: Analyze High Level Synthesis.

Introduction to VLSI Design

Automation, use of VLSI CAD tools, Algorithmic Graph Theory, Computational Complexity and ROBDD; Partitioning and Placement: KL algorithm, FM algorithm, Group-migration algorithm, Simulated Annealing and Evolution

Floor planning and Pin Assignment

Placement, Layout styles, Discrete methods in global placement, Timing-driven placement, Routing: Global Routing, detailed routing, Graph models, Line Search, Maze Routing, Channel Routing, Steiner Tree based Algorithms, ILP base approaches

Performance Issues in circuit layout

delay models, timing driven placements, timing driven routing, Via Minimization, Over the Cell Routing – Single layer and Two layer routing, Clock and Power Routing

Compaction

Problem formulation, One Dimension compaction, Two Dimension compaction, Hierarchical Compaction, Compaction Algorithms. Physical Design Automation in FPGAs

High level synthesis

Introduction to HDL, HDL to DFG, operation scheduling: constrained and unconstrained scheduling, ASAP, ALAP, List scheduling, Force directed Scheduling, operator binding, Static Timing Analysis: Delay models, setup time, hold time, cycle time, critical paths, Topological MVS Logical timing analysis, False paths, Arrival time (AT), Required arrival Time (RAT), Slacks

Text Books :

1 .Sherwani, N., Algorithms for VLSI Physical Design Automation, Springer (2005) 3rded

2. Gerez S.H., Algorithms for VLSI Design Automation, John Wiley (1998

Reference Books :

1 .Sarrafzadeh, M. and Wong, C. K., An Introduction to VLSI Physical Design, McGraw Hill (1996).

2.Sait, S. M. and Youssef, Habib, VLSI Physical Design Automation – Theory and Practice, World Scientific, 2004.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

CAD FOR VLSI (CV)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 954 (Professional Elective – III)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO 1; Understand the basic knowledge of unix commands and programming skills.

CO2; Analyze the programming model of perl and python.

CO3:Analyze programs in perl and python

CO4:Analyze case studies in python operations

Introduction to UNIX

Architecture, Basic commands, General Purpose utilities, File System, Handling Files, File Attributes, vi editor, regular expression, shell scripting.

PERL

Introduction to Perl, Literals, Variable types and contexts, Perl Arrays, Perl Hashes, Operators, Conditionals, Loops & Subroutines, Files and File handling.

DIRECTORY

Directory, Pattern Matching and Regular Expressions, Accessing System Resources, Generating Reports with Perl

PYTHON

Introduction to Python, Fundamentals to Python, operators and conditions, regular expressions, Loops, working with files, Arguments, modules.

LABORATORY WORK

Writing basic commands in unix, perl and python. Also write programs in unix, perl and python.

Text Books :

1. Sumitbha Das, Unix: Concepts And Applications, McGraw Hill Education, 4th edition.
2. Ellie Quigley, Perl by Example, Prentice Hall, 5th edition, 2014
3. Mark Lutz, Learning Python, O'Reilly Media, 5th edition, 2013.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

MIXED SIGNAL CIRCUIT DESIGN (MSCD)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	**Hours/Week**			**Credits**	**Maximum Marks**		
EC 955 (Professional Elective – III)	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
	3	**-**	**-**	**3**	**40**	**60**	**100**
Sessional Exam Duration : 2 Hrs					**End Exam Duration: 3 Hrs**		

Course Outcomes : At the end of the course the student will be able to

CO1: Analyze mathematics, science, and engineering to design CMOS analog circuits to achieve performance specifications.

CO2: Analyze formulates, and solves engineering problems in the area of mixed-signal design.

CO3: Use the techniques and skills for design and analysis of CMOS based switched capacitor circuits.

CO4: Analyze a mixed-signal integrated circuit.

Introduction

Device Models, IC Process for Mixed Signal, Concepts of MOS Theory.

Comparators & Data Convertors

Circuit Modeling, Auto Zeroing Comparators, Differential Comparators, Regenerative Comparators, Fully Differential Comparators, Latched Comparator, Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL

High Speed A/D & D/A Converter Architectures

Flash, Folding, Interpolating, piplelined, Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converters.

Implementation and Design of High Performance A/D and D/A Converters

System Design, Digital Compensation, Noise, and Mismatch, Layout and Simulation Technologies for Data Converters.

Advanced topics

Multipliers, Oscillators, Mixers, Passive Filter Design, Active filter design, Switched Capacitor Filters, Frequency Scaling, Phase-Locked Loops, Device Modeling for AMS IC Design, Concept of AMS Modeling and Simulation

Text Books :

1 . Baker, R.J., Li, H.W. and Boyce, D.E., CMOS: Circuit Design, Layout and Simulation, IEEE Press (2007) 2nd ed.

2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, Wiley (2002).

3.Jespers, P.G. A., Integrated Converters: D-A and A-D Architectures, Analysis and Simulation, Oxford University Press (2001).

Reference Books :

1.Plassche, Rudy J.Van De, Integrated A-D and D-A Converters, Springer (2007), 2nd ed.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

EMBEDDED NETWORKS AND PROTOCOLS (ENP)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 956 (Professional Elective – IV)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand concepts of CAN protocols and Ethernet

CO2: Understand elements of a network.

CO3: Analyze industrial networking protocols.

CO4: Analyze RF communication

INTRODUCTION TO CAN

The CAN bus - General - Concepts of bus access and arbitration - Error processing and management - From concept to reality -Patents, licenses and certification – CAN protocol: 'ISO 11898-1'- Content of the different ISO/OSI layers of the CAN bus-Compatibility of CAN 2.0A and CAN 2.0B.

ETHERNET BASICS

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

EMBEDDED ETHERNET

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

INDUSTRIAL NETWORKING PROTOCOL

LIN – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus – Audiovideo buses - I2C Bus - D2B

RF COMMUNICATION

Radio-frequency communication: internal and external - Remote control of opening parts - PKE (passive keyless entry) and passive go- TPMS (tyre pressure monitoring systems) -Wireless networks GSM-Bluetooth - IEEE 802.11x - NFC (near-field communication).

Text Books :

1 .*Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire*, Dominique Paret,John Wiley & Sons Ltd- 2007.

2. *Embedded Ethernet and Internet Complete*, Jan AxelsonPenram publications

Reference Books :

1. *Embedded networking with CAN and CAN open*,.GlafP.Feiffer, Andrew Ayre and Christian Key old Embedded System Academy 2005

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN (MESD)

II Semester :VLSI & ES					**Scheme : 2022**		
Course Code	**Hours/Week**			**Credits**	**Maximum Marks**		
EC 957 (Professional Elective – IV)	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exam**	**TOTAL**
	3	**-**	**-**	**3**	**40**	**60**	**100**
Sessional Exam Duration : 2 Hrs					**End Exam Duration: 3 Hrs**		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand ARM Architecture and pipelining.

CO2: Analyze ARM processor instruction set and thumb formats.

CO3: Use ARM programming model to frame programs

CO4: Analyze the memory management and cache issues of ARM processor

ARM Architecture

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

ARM Programming Model – I

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

ARM Programming Model – II

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack

ARM Programming

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditions.

Memory Management

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Text Books :

1 .ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier

Reference Books :

1.Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

PRINCIPLES OF DISTRIBUTED EMBEDDED SYSTEMS (PDES)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 958 (Professional Elective – IV)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand C language and assembly programming

CO2: Understand Object orientation for programming and C++

CO3: Analyzesoftware modeling fundamentals.

CO4: Analyze embedded software development tools

REAL-TIME ENVIRONMENT

Real-time computer system requirements – classification of real time systems – simplicity – global time – internal and external clock synchronization – real time model. Real – time communication – temporal relations – dependability – power and energy awareness – real –time communication – event triggered – rate constrained – time triggered

REAL-TIME OPERATING SYSTEMS

Inter component communication – task management – dual role of time – inter task interactions – process input/output – agreement protocols – error detection

SYSTEM DESIGN

Scheduling problem - static & dynamic scheduling – system design – validation – time–triggered architecture

INTRODUCTION TO CAN

Introduction to CAN Open – CAN open standard – Object directory – Electronic Data Sheets & Devices.

CAN STANDARDS

Configuration Files – Service Data Objectives – Network management CAN open messages – Device Profile Encoder

Text Books :

1 .HermannKopetz, “Real–Time systems – Design Principles for distributed Embedded Applications”, 2nd Edition, Springer 2011.

Reference Books :

1GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Copperhill Media Corporation, 2008.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

VLSI DESIGN FOR TESTABILITY (VDFT)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 959 (Professional Elective – V)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand all the levels of testing done in VLSI circuits

CO2: Understand the DFT principles in VLSI circuits

CO3: Analyze logic and fault simulation in VLSI circuits

CO4: Analyze test generation in VLSI circuits

Introduction to Testing

Importance of Testing, Testing During the VLSI Lifecycle, Challenges in VLSI Testing- Challenges in VLSI Testing, Fault Models; Levels of Abstraction in VLSI Testing.

Design for Testability

Introduction, Testability Analysis----SCOAP Testability Analysis, Probability-Based Testability Analysis, Simulation-Based Testability Analysis

Logic and Fault Simulation

Logic Simulation for Design Verification, Fault Simulation for Test and Diagnosis, Simulation Models-Gate-Level Network, Logic Symbols, Logic Element Evaluation

Test Generation

Introduction, Random Test Generation, Boolean difference, untestable faults, Designing a Stuck-At ATPG for Combinational Circuits--- A Naive ATPG Algorithm, A Basic ATPG Algorithm, D Algorithm, PODEM.

Logic Built-In Self-Test

Introduction, Test Pattern Generation--- Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing; Output Response Analysis--- Ones Count Testing, Transition Count Testing, Signature Analysis, Logic BIST Architectures

Text Books :

1 .Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, “VLSI Test Principles and Architectures: Design for Testability”, 1st Edition, Morgan Kaufmann, 2006.

Reference Books :

1.M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers, 2000

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

VLSI SIGNAL PROCESSING (VS)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 960 (Professional Elective – V)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Apply the principles of DFG in DSP architectures

CO2: Apply pipelining and parallel processing on FIR and IIR systems to achieve high speed and Lowpower

CO3: Solve Register minimization, retiming, folding techniques for the given digital filter.

CO4: Understand the overview FIR filter Systolic architecture design.

Introduction to Digital Signal Processing Systems

Introduction, Typical DSP Algorithms, DSP Application demands and scaled CMOS technologies, Representation of DSP Algorithms.

Iteration Bound

Introduction, Data Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs.

Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power

Retiming , Folding and Unfolding

Introduction, Definitions and properties, Solving systems of inequalities, Retiming Techniques, An algorithm for unfolding, Critical path. Introduction, Folding techniques, Register minimization techniques, Register minimization in folded architecture, Folding of multirate systems. Unfolding and retiming, Applications of unfolding.

Systolic Architecture Design

Introduction, System array design methodology, FIR systolic arrays, selection of scheduling vector, Matrix-matrix multiplication and 2-D systolic array design, Systolic Design for space representations containing delays.

Text Books :

1 .Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, WileyInter Science. 1998.

2.Kung S. Y, H. J. While House, T. Kailath, *VLSI and Modern Signal processing*, Prentice Hall, 1985.

Reference Books :

1 Jose E. France, YannisTsividis, Design of Analog, Digital VLSI Circuits for Telecommunications and Signal Processing, Prentice Hall,1994.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

MEMORY DESIGN AND TESTING (MDT)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
EC 961 (Professional Elective – V)	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	3	-	-	3	40	60	100
Sessional Exam Duration : 2 Hrs					End Exam Duration: 3 Hrs		

Course Outcomes : At the end of the course the student will be able to

CO1: Understand Basics of memory chip Design and Technology.

CO2: AnalyzeRAM and DRAM Design.

CO3: Analyze On-Chip Voltage Generators.

CO4: Interpret Laplace Trans., CTFT and DTFT.

CO5: Analyze High-Performance Subsystem Memories

Introduction to Memory Chip Design

Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology.

Basics of RAM Design and Technology& DRAM

Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law,High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.

On-Chip Voltage Generators

Substrate-Bias Voltage (VBB) Generator, Voltage Up Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.

High-Performance Subsystem Memories

Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.

Ultra-Low-Voltage Memory Circuits

Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.

Text Books :

1.Itoh, K., VLSI Memory Chip Design, Springer (2006).

2.Sharma, A. K., Semiconductor Memories: Technology, Testing and Reliability, Wiley- IEEE press (2002).

3.Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002).

4.Sharma, A. K., Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley (2002).

5.Prince, B., Semiconductor Memories: A handbook of Design, Manufacture and Application, John Wiley (1996) 2nd ed.

Reference Books :

1.Plassche, Rudy J.Van De, Integrated A-D and D-A Converters, Springer (2007), 2nd ed.

Question Paper Pattern:

Internal Assessment: The question paper shall consist of **Six** questions out of which the student shall answer any **Four** questions

End Exam: The question paper shall consist of **Eight** questions out of which the student shall answer any **Five** questions

List of Audit Courses

Description	Subject Title
Audit Course – II	Pedagogy Studies
	Personality Development through Life Enlightenment Skills
	Stress Management by Yoga

PEDAGOGYSTUDIES
(Audit Course – II for M. Tech-II Semester)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
AU 102	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	0	-	-	-

Course Outcomes : At the end of the course the student will be able to

CO1: What pedagogicalpracticesarebeingusedbyteachersinformalandinformalclassroomsin Developing countries?

CO2: Whatistheevidenceontheeffectivenessofthesepedagogicalpractices,inwhatconditions, And with what population of learners?

CO3: Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand Guidance materials best support effective pedagogy?

UNIT - I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, search questions**.** Overview of methodology and Searching.

UNIT - II

Thematic Overview Pedagogicalpracticesarebeingusedbyteachersinformalandinformalclassroomsin developing countries. Curriculum,Teacher education.

UNIT - III

Pedagogical Practices and Methodology Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitude and beliefs and Pedagogic strategies.

UNIT - IV

Professional Development: Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

UNIT - V

Research Gaps and Future Directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

Text Books :

1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare,31(2):245-261.

2. AgrawalM(2004) curricular for min schools: The importance of evaluation, Journal of Curriculum Studies,36 (3):361-379.

Reference Books :

1. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project(MUSTER)countryreport1.London:DFID.

2. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International JournalEducationalDevelopment,33 (3):272–282.

PERSONALITYDEVELOPMENT THROUGHLIFEENLIGHTENMENT SKILLS
(Audit Course – IIfor M. Tech-II Semester)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
AU 102	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	0	-	-	-

Course Outcomes : At the end of the course the student will be able to

CO1: Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and Achieve the highest goal in life

CO2: The person who has studied Geeta will lead the nation and mankind to peace and prosperity

CO3: Study of Neetishatakam will help in developing versatile personality of students

UNIT - I

Neetisatakam-Holistic development of personality

- Verses-19,20,21,22(wisdom)
- Verses-29,31,32(pride&heroism)
- Verses-26,28,63,65(virtue)

UNIT - II

Neetisatakam-Holistic development of personality

- Verses-52,53,59(dont's)
- Verses-71,73,75,78(do's)

UNIT -III

Approach to day to day work and duties.

- ShrimadBhagwadGeeta: Chapter2-Verses41, 47,48,
- Chapter3-Verses13,21, 27, 35,Chapter6-Verses5,13,17, 23, 35,
- Chapter18-Verses45,46,48.

UNIT - IV

Statementsofbasicknowledge.

- ShrimadBhagwadGeeta:Chapter2-Verses56,62,68
- Chapter12-Verses13,14,15,16,17,18

UNIT - V

Personality of Role model. Shrimad BhagwadGeeta:

- Chapter2-Verses17,
- Chapter3-Verses36,37,42,
- Chapter4-Verses18, 38,39
- Chapter18–Verses37,38,63

Text Books :

1. "SrimadBhagavadGita"by SwamiSwarupanandaAdvaitaAshram(PublicationDepartment),Kolkata.

Reference Books :

1. Bhartrihari'sThreeSatakam(Niti-sringar-vairagya)byP.Gopinath,RashtriyaSanskritSansthanam,NewDelhi.

STRESS MANAGEMENT BY YOGA
(Audit Course – II for M. Tech-II Semester)

II Semester :VLSI & ES					Scheme : 2022		
Course Code	Hours/Week			Credits	Maximum Marks		
AU 102	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
	2	-	-	0	-	-	-

Course Outcomes : At the end of the course the student will be able to

CO1: Develop healthy mind in a healthy body thus improving social health also

CO2: Improve efficiency

UNIT - I

Definitions of Eight paths of yog.(Ashtanga)

UNIT -II

Yam and Niyam.

UNIT - III

Do`s and Don'ts in life.

i) Ahinsa, satya, astheya,bramhacharya and aparigraha

ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT - IV

Asanand Pranayam

UNIT - V

i) Various yog poses and their benefits for mind&body

ii) Regularization of breathing techniques and its effects-Types of pranayam

Text Books :

1. 'Yogic Asanas for Group Training-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur

Reference Books :

1. "RajayogaorconqueringtheInternalNature"bySwamiVivekananda,AdvaitaAshrama (Publication Department) ,Kolkata