G. PULLA REDDY ENGINEERING COLLEGE (Autonomous): KURNOOL

Accredited by NBA of AICTE and NAAC of UGC with A Grade,

Affiliated to JNTUA, Anantapuramu

SCHEME – 2025

Scheme and Syllabus for I, II, III, IV Semesters of

Two-year M. Tech. Degree Programme in

VLSI & Embedded Systems

TWO YEAR M. Tech DEGREE PROGRAMME

Scheme of Instruction and Examination

(Effective for the students admitted from the academic year 2025-26 onwards)

M.Tech I Semester – VLSI and Embedded Systems (VLSI & ES) Scheme – 2025

S. No.	Category	Course Title	L	T	P	Credits	CIA Marks	End Exam Marks	Total
I		**Theory**							
1.	PC	CMOS Digital IC Design	3	0	0	3	40	60	100
2.	PC	Micro controllers and Programmable Digital Signal Processors	3	0	0	3	40	60	100
3.	PE	Professional Elective – I	3	0	0	3	40	60	100
4.	PE	Professional Elective – II	3	0	0	3	40	60	100
5.	MC	Research Methodology & IPR	2	0	0	2	100	-	100
6.	SE	RTL Synthesis, Simulation and Verification	0	1	2	2	40	60	100
7.	AC	Audit Course - I	2	0	0	0	-	-	-
II		**Practical**							
8.	PCL	CMOS Digital IC Design Lab	0	0	4	2	40	60	100
9.	PCL	Micro Controllers and Programmable Digital Signal Processors Lab	0	0	4	2	40	60	100
						20	**380**	**420**	**800**

M.Tech II Semester – VLSI and Embedded Systems (VLSI & ES) Scheme – 2025

S. No.	Category	Course Title	L	T	P	Credits	CIA Marks	End Exam Marks	Total
I		**Theory**							
1.	PC	CMOS Analog IC Design	3	0	0	3	40	60	100
2.	PC	Embedded Systems for Internet of Things	3	0	0	3	40	60	100
3.	PE	Professional Elective – III	3	0	0	3	40	60	100
4.	PE	Professional Elective – IV	3	0	0	3	40	60	100
5.	MC	Quantum Technologies And Applications	2	0	0	2	40	60	100
6.	PC	Comprehensive Viva Voce	0	0	0	2	-	100	100
7.	AC	Audit Course - II	2	0	0	0	-	-	-
II		**Practical**							
8.	PCL	CMOS Analog IC Design Lab	0	0	4	2	40	60	100
9.	PCL	Embedded IoT Lab	0	0	4	2	40	60	100
						20	**280**	**520**	**800**

** **Students have to undergo an industry internship after First year II Semester for duration of 6 to 8 Weeks**.

TWO YEAR M. TECH DEGREE PROGRAMME

Scheme of Instruction and Examination

(Effective for the students admitted from the academic year 2025-26 onwards)

M.Tech III Semester – VLSI and Embedded Systems (VLSI & ES) Scheme – 2025

S. No.	Category	Course Title	L	T	P	Credits	CIA Marks	End Exam Marks	Total
1.	PE	Professional Elective-V	3	0	0	3	40	60	100
2.	OE	Open Elective (OE) *	3	0	0	3	40	60	100
3.	PR	Dissertation Phase – I	0	0	20	10	100	-	100
4.		Industry Internship	0	0	0	2	100	-	100
5.	CAA	Co – Curricular Activities	0	0	0	1	100	-	100
	Total					**19**	**380**	**120**	**500**

***Open Elective through MOOCs**

M.Tech IV Semester – VLSI and Embedded Systems (VLSI & ES) Scheme – 2025

S. No.	Category	Course Title	L	T	P	Credits	CIA Marks	End Exam Marks	Total
1	PR	Dissertation Phase – II	0	0	**16**	**8**	**100**	**-**	**100**
2	PR	Project Viva - Voce	-	-	**-**	**8**	**-**	**100**	**100**
	Total					**16**	**100**	**100**	**200**

List of Professional Elective Courses

Description	Subject Title
PE – I	Hardware Algorithms for Computer Arithmetic(HACA)
	Scripting Languages for VLSI (SLV)
	Advanced Digital System Design Using Verilog (ADSD)
PE – II	Embedded Programming (EP)
	Embedded System Architecture (ESA)
	Hardware Software Co-design (HSC)
PE – III	RFIC Design
	Physical Design Automation(PDA)
	Mixed Signal Circuit Design(MSCD)
PE – IV	SOC Architecture
	Embedded Networks and Protocols (ENP)
	Principles of Distributed Embedded Systems (PDES)
PE – V	VLSI Signal Processing (VS)
	Pattern Recognition and Machine Learning(PRM)
	Industrial Internet of Things

List of Audit Courses

Description	Subject Title
Audit Course – I	English for Research Paper Writing
	Disaster Management
	Essence of Indian Traditional Knowledge

Open Elective

OE	IOT and Its Applications

CMOS DIGITAL IC DESIGN (CDICD)

M.Tech I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC851	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2Hrs						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Demonstrate the operation and characteristics of Pseudo NMOS and CMOS inverters, including threshold voltage, gain, and transient response.

CO2: Design and analyze combinational MOS logic circuits using NMOS, CMOS, and transmission gate logic for realizing Boolean expressions.

CO3: Construct sequential MOS logic circuits such as latches and flip-flops using CMOS technology.

CO4: Evaluate the working principles and performance of dynamic logic circuits including voltage bootstrapping and dynamic CMOS logic.

CO5: Analyze the organization and operation of semiconductor memories such as DRAM, SRAM, and Flash memory and analyze their characteristics.

UNIT – I

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT – II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT – III

Sequential MOS Logic Circuits: Behaviour of Bi-stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT – IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT – V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

References:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

Press, 2011

2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS (MDSP)

M.Tech I Semester: VLSI &ES						Scheme: 2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC852	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration: 3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Learn about ARM Microcontroller architectural features

CO2: Understand the ARM 'C' Programming for various applications

CO3:Understand the peripheral operations of LPC Microcontrollers

CO4: Understand the DSP processor Architectures and processor family

CO5: Understand the DSP processor instruction set, programming & development tools

UNIT – I

ARM Cortex-Mx Processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

UNIT – II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT – III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT – IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT – V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2ndEdition.

References:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on Arm - www.arm.com, NXP Semiconductor - www.nxp.com and Texas Instruments - www.ti.com

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

HARDWARE ALGORITHMS FOR COMPUTER ARITHMETIC (HACA)

M.Tech I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC853	PE-1	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration: 3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Understand the Redundant number systems

CO2: Analyze Algorithms for fast addition

CO3: Analyze VLSI implementation aspects, High speed multiplication

CO4: Interpret Algorithms for fast division and impact of hardware technology

CO5: Understand the Programming Models And Development Tools

UNIT – I

Algorithms for Fast Addition :Basic Addition and Counting, Bit-serial and ripple-carry adders, Addition of a constant: counters, Manchester carry chains and adders, Carry-Look-ahead Adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in Fast Adders, Simple carry-skip and Carry-select adders, Hybrid adder designs, Optimizations in fast adders, Multi-Operand Addition, Wallace and Dadda trees, Parallel counters, Generalized parallel counters, Adding multiple signed numbers.

UNIT – II

High-Speed Multiplication: Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers, VLSI layout considerations.

UNIT – III

Fast Division and Division Through Multiplication: Basic Division Schemes, Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, HighRadix Dividers, Variations in Dividers, Combined multiply/divide units, Division by Convergence, Hardware implementation.

UNIT – IV

Digital Input, Output, and Displays: Square-Rooting Methods, The CORDIC Algorithms, Computing algorithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by Table Lookup, Tradeoffs in cost, speed, and accuracy.

UNIT – V

Function Evaluation :Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I2C.

Textbooks:

1 .Parhami, B., Computer Arithmetic: Algorithms and Hardware Design, Oxford University Press (2000).

2. Ercegovac, M. and Lang, T., Digital Arithmetic, Elsevier (2005).

References:

1 .Koren, I., Computer Arithmetic Algorithms, 2nd Edition, Uni Press (2005) 2nd ed.

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

SCRIPTING LANGUAGES FOR VLSI (SLV)

I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC854	PE-1	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration: 3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Scripting the given code in HDLs

CO2: Utilize Scripting languages in their projects.

CO3: Understand the subroutines and functions

CO4: Understand the process ,thread model and debugger

CO5: Analyze and functional verification using UVM, Java Script, SKILL etc.

UNIT – I

Overview of scripting languages: PERL, File handles, Operators, Control structures, Regular expressions, Built in data types, Operators, Statements and declarations- simple, Compound, Loop statements, Global and scoped declarations

UNIT – II

. **Pattern matching:** Regular expression, Pattern matching operators, Character classes, Positions, capturing and clustering.

UNIT – III

Subroutines : Syntax, Semantics, Proto types, Format variables, References, Data structures, Arrays of arrays, Hashes of arrays, Hashes of functions, Inter process communication, Signals, Files, Pipes, sockets.

UNIT – IV

Threads: Process model, Thread model, Perl debugger, Using debugger commands, Customization, Internals and externals, Internal data types, Extending perl, embedding perl, Exercises for programming using perl.

UNIT – V

Universal Verification Methodology(UVM): System and functional verification using UVM(Universal Verification Methodology), SKILL, CGI, java script, VB script

Textbooks/References:

1. Larry Wall, Tom Christiansen, John Orwant, *Programming perl*, 3rd Edition, Oreilly publications
2. Randal L, Schwartz Tom Phoenix, *Learning PERL*, Oreilly publications

Online Resources:

www.cadence.com(UVM) , www.accellera.org (standard UVM)

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

ADVANCED DIGITAL SYSTEM DESIGN USING VERILOG (ADSD)

M. Tech I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC 855	PE-I	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration: 3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Analyze and design sequential digital circuits

CO2: Analyze and design asynchronous sequential digital circuits

CO3: Design using programmable logic devices

CO4: Identify the requirements and specifications of the system required for a given application

CO5: Design and use programming tools for implementing digital circuits of industry standards

UNIT – I

Sequential Circuit Design: Analysis of clocked synchronous sequential circuits and modeling-State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM.

UNIT – II

Asynchronous Sequential Circuit Design: Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.

UNIT – III

Fault Diagnosis and Testability Algorithms: Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.

UNIT – IV

Synchronous Design Using Programmable Devices: Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

UNIT – V

System Design Using Verilog : Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

Textbooks:

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001

References:

1. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
2. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
3. M.D.Ciletti ,Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.

4. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

EMBEDDED PROGRAMMING (EP)

M.Tech I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC856	PE-II	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration: 3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Analyze the variation of C language and assembly language programming

CO2: Apply the basics for programming in C

CO3: Utilize Object orientation for programming and C++

CO4: Apply software modelling fundamentals

CO5: Analyze Embedded software development tools

UNIT – I

Introduction to Assembly language and data representation in C: Assembly language programming – macros - Data representation – Twos complement, fixed point and floating point number formats –Low level programming in C: Primitive data types – Pointers –Structures – Unions – Dynamic memory allocation – Functions – recursive functions - Linked lists.

UNIT – II

Programming in C : Register usage conventions – Typical use of addressing options – Instruction sequencing – Procedure call and return – Functions – recursive functions – 8, Parameter passing – Retrieving parameters – Everything in pass by value – Temporary variables – threads – pre-emptive kernels – system timer – scheduling

UNIT – III

Object Oriented Programming : Object oriented analysis and design - C++ classes and objects – functions – data structures – examples

UNIT – IV

Unified modeling language: Connecting the object model with the use case model – Key strategies for object identification – UML basics. Object state behaviour – UML state charts – Role of scenarios in the definition of behaviour – Timing diagrams – Sequence diagrams – Event hierarchies – types and strategies of operations – Architectural design in UML concurrency design – threads in UML

UNIT – V

Embedded software development tools and RTOS : The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS

Textbooks:

1. David E. Simon, " *An Embedded Software Primer*", Pearson Education, 2003
2. Daniel W. Lewis, " Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.

References:

1. Steve Heath, " *Embedded system design*", Elsevier, 2003.
2. E. Balaguruswamy, " *Object oriented programming with C++*", Tata McGraw Hill, 2011.

Question Paper Pattern:

Sessional Exam: The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Exam: The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

EMBEDDED SYSTEM ARCHITECTURES (ESA)

M.Tech I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC857	PE-II	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration: 3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Understand the Embedded System Models

CO2: Analyze the Hardware components of Embedded systems

CO3: Interpret rationale and concepts for designing embedded systems

CO4: Analyze the Embedded Issues of Software

CO5: Analyze the typical engineering issues of software development

UNIT – I

Introduction to embedded systems : Embedded system model – embedded standards – block diagrams – powering the hardware – embedded board using Von Neuman model. Embedded processors: ISA architecture models – application specific ISA models – general purpose ISA models – instruction level parallelism.

UNIT – II

Processor Hardware : Internal processor design: ALU – registers – control unit – clock – on chip memory – processor i/o – interrupts – processor buses – processor performance.

UNIT – III

Support Hardware : Board memory: ROM – RAM – cache – auxiliary memory – memory management memory performance – board buses: arbitration and timing – PCI bus example integrating bus with components – bus performance

UNIT – IV

Software : Middleware and applications: PPP – IP middleware – UDP – Java .application layer: FTP client SMTP– HTTP server and client

UNIT – V

Engineering Issues of Software : Design and development: architectural patterns and reference models – creating the architectural structures – documenting the architecture – analyzing and evaluating the architecture – debugging testing, and maintaining

Textbooks:

1. Embedded system architecture, Tammy Noergaard, Elsevier, 2006.

References:

1. Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C, Jean J. Labrosse, The publisher, Paul Temme, 2011.

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

HARDWARE SOFTWARE CO-DESIGN (HSC)

M.Tech I Semester: VLSI &ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC858	PE-II	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	40	60	100
Sessional Exam Duration: 2 Hrs					End Exam Duration:3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

CO1: Understand H/W and S/W Co Design models.

CO2: Understand H/W and S/W prototyping and target architectures

CO3: Apply compilation techniques and tools suitable for embedded processor architectures.

CO4: Analyze H/W and S/W design specifications and verification

CO5: Analyze the H/W and S/W system level synthesis

UNIT – I

Co-Design Issues: Co-Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware–software partitioning distributed system co-synthesis

UNIT – II

Prototyping and Emulation: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment

UNIT – IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT – V

Languages for System – Level Specification and Design-I, II: System – level specification, design representation for system level synthesis, system level specification languages. Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Textbooks:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

References:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

Question Paper Pattern:

Sessional Examination:

The Sessional examination question paper shall be for **30 marks**. The question paper shall consist of three questions, and student must answer all three questions (without choice). Each question carries 10 marks.

End Examination:

The End examination question paper shall be for **60 marks**. Two questions of EITHER/OR type shall be framed from each unit. Each question may contain sub-questions. Students shall answer any one question from each unit, i.e., a total of five questions, with each question carrying 12 marks.

RESEARCH METHODOLOGY & IPR (RM & IPR)

M.Tech I Semester: Common for all branches						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
MC101	MC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		2	0	0	2	100	-	-
Sessional Exam Duration: 2 Hrs						End Exam Duration:-		

Course Outcomes:

After the completion of the course students will be able to

CO1: Understand overview of research process, state the research problem and conduct a literature review of the concepts comprising the research questions

CO2: Study the data collection methods and process the data statistically.

CO3: Apply multivariate analysis and experimental research methods for reliable data interpretation

CO4: Understand the principles , types and global framework of Intellectual property rights

CO5: Explain the patent process, filing procedures and legal aspects of intellectual property

UNIT – I

Fundamentals of Research Methodology: Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

UNIT – II

Data Collection and Sources: Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

UNIT – III

Data Analysis and Reporting: Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

UNIT – IV

Understanding Intellectual Property Rights: Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT – V

Patents : Objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

Text Books :

1. Stuart Melville and Wayne Goddard, *Research Methodology: An introduction for Science & Engineering students*, Juta and Company Ltd, 2004
2. Catherine J. Holland, *Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets*, Entrepreneur Press, 2007.

Reference Books:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar , *Research Methodology: A Step-by-Step Guide for Beginners.* . David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
3. Deborah E. Bouchoux , *Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition,* Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, *The Craft of Research*, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.
6. Peter Elbow, *Writing With Power*, Oxford University Press, 1998.

Online Resources (Free & Authentic):

1. **Coursera / edX** – Research Methodology and Data Analysis courses
2. **Springer Link & Science Direct** – Latest journals on research design and statistics
3. **Google Scholar** – Free access to research papers
4. **NCBI Bookshelf** – Open-access research methodology resources
5. **Khan Academy (Statistics & Probability)** – For fundamentals of hypothesis testing, regression, and ANOVA.

RTL SYNTHESIS, SIMULATION AND VERIFICATION (RSSV)

M. Tech I Semester-VLSI & ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
SEC	SE	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		0	1	2	2	40	60	100
Sessional Exam Duration:2 Hrs						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Demonstrate the process steps required for simulation /synthesis.

CO2: Design and simulate various combinational and sequential circuits using HDL.

CO3: Develop an RTL code for various real time applications.

CO4: Synthesize / Simulate an RTL code for several digital designs.

CO5: Build and verify various digital circuits.

LIST OF EXPERIMENTS

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (System Verilog/VHDL basics).
- **Lab:**
  1. Write synthesizable Verilog /System Verilog code for:
     a) Half Adder, Full Adder
     b) 4-bit Ripple Carry Adder
     c) 4-bit Synchronous Counter (Up/Down)
  2. FSM Design: Sequence Detector (e.g., detect “1011”).

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- **Lab:**
  1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
  2. Generate gate-level netlist and analyze area, delay, power reports.
  3. Apply constraints (clock, timing) and observe impact on synthesis results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Test bench creation, waveforms, debugging.
- **Lab:** Run simulations
  1. Develop test benches for:
     a) 4-bit ALU (add, sub, AND, OR).
     b) Universal Shift Register.
  2. Perform functional simulation using EDA tools
  3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- **Lab:** Writing simple verification test benches.
  1. Write self-checking test benches for combinational and sequential circuits.
  2. Use assertion-based verification (System Verilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
  3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- **Lab:** Design, synthesize, simulate, and verify a **digital subsystem** such as:

  1. UART Transmitter/Receiver
  2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
  3. FIFO Buffer with full/empty flags

Textbooks :

1. Samir Palnitkar – *Verilog HDL: A Guide to Digital Design and Synthesis*.
2. Michael Ciletti – *Advanced Digital Design with the Verilog HDL*.
3. Chris Spear & Greg Tumbush – *SystemVerilog for Verification*.
4. David Rich – *Design and Verification with SystemVerilog*

References :

1. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx, 2011.
3. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books, 2002

ENGLISH FOR RESEARCH PAPER WRITING (ERPW)

(Audit Course – I for M. Tech-I Semester)

M.Tech I Semester: Common for all branches						Scheme: 2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
AC101	AC-I	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		2	0	0	0	-	-	-

Course Outcomes:

After the completion of the course students will be able to

CO1: Recall the key language aspects and structural elements of academic writing in research papers.

CO2: Explain the importance of clarity, precision, and objectivity in research writing.

CO3: Apply critical reading strategies and advanced grammar skills to analyze and write research papers.

CO4: Analyze research articles and identify the strengths and limitations of different methodologies.

CO5: Evaluate the effectiveness of different language and technology tools in research writing, including AI- assisted tools and plagiarism detection software.

CO6: Develop a well-structured research paper that effectively communicates complex ideas.

UNIT – I

Fundamentals of Academic English:

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT – II

Reading Skills for Researchers:

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT – III

Grammar Refinement for Research Writing:

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active-Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT – IV

Mastery in Refining Written Content/Editing Skills:

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

UNIT – V

Technology and Language for Research:

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

Textbooks:
1.Bailey. S. A*cademic Writing: A Handbook for International Students.* London and New York: Routledge,2015.
2. Adrian Wallwork, *English for Writing Research Papers*, Springer New York Dordrecht Heidelberg London, 2011.
References:
1. Craswell, G. *Writing for Academic Success,* Sage Publications, 2004.
2. Peter Elbow, *Writing With Power, E-book*, Oxford University Press, 2007
3. Oshima, A. & Hogue, A. *Writing Academic English*, Addison-Wesley, New York, 2005
4. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5.Goldbort R.*Writing for Science*, Yale University Press (available on Google Books), 2006
6. Day R.*How to Write and Publish a Scientific Paper*, Cambridge University Press, 2006
Online Learning Resources:
1. https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/ 2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview 3. "Writing in the Sciences" – Stanford University (MOOC on Coursera) (https://www.coursera.org/learn/sciwrite) 4. Academic Phrasebank – University of Manchester (http://www.phrasebank.manchester.ac.uk) 5. OWL (Online Writing Lab) – Purdue University, (https://owl.purdue.edu) *(Resources on APA/MLA formats, grammar, structure, paraphrasing)* 6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources.

DISASTER MANAGEMENT (DM)

(Audit Course – I for M. Tech-I Semester)

M. Tech I Semester: Common for all branches						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
AC102	AC-1	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		2	0	0	0	-	-	-

Course Outcomes:

After the completion of the course students will be able to

CO1: Define and distinguish between hazards and disasters, and explain their types, nature, and impacts.

CO2: Assess the economic, social, and ecological repercussions of major natural and man-made disasters.

CO3: Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness.

CO4: Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels.

CO5: Formulate and evaluate structural and non-structural disaster mitigation strategies, with emphasis on Indian programs and emerging trends.

UNIT – I

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT – II

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters : Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT – III

Disaster Preparedness and Management: Preparedness :Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness

UNIT – IV

Risk Assessment: Disaster Risk- Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment .Strategies for Survival.

UNIT – V

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Textbooks:

1. Gupta, H. K. *Disaster Management*. Universities Press, 2003
2. Singh, R. B. *Natural Hazards and Disaster Management*. Rawat Publications, 2006.

References:

1. Coppola, D. P. (2020). *Introduction to International Disaster Management* (4th ed.). Elsevier.
2. Shaw, R., & Izumi, T. (2022). *Science and Technology in Disaster Risk Reduction in Asia*. Springer.
3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). *Handbook of Hazards and Disaster Risk Reduction and Management* (2nd ed.). Routledge.
4. Saini, V. K. (2021). *Disaster Management in India: Policy, Issues and Perspectives*. Sage India.
5. Kelman, I. *Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes,* Oxford University Press, 2022
6. Sahni, P. & Dhameja, A. *Disaster Mitigation: Experiences and Reflections*. Prentice Hall of India, 2004.

Online Resources :

1. **National Disaster Management Authority (NDMA), India**: https://ndma.gov.in – official guidelines, reports, and policy frameworks.
2. **United Nations Office for Disaster Risk Reduction (UNDRR)**: https://www.undrr.org – Sendai Framework, global risk reduction strategies.
3. **Global Disaster Alert and Coordination System (GDACS)**: https://www.gdacs.org – real-time disaster alerts.
4. **World Health Organization (WHO)** – https://www.who.int/emergencies – disaster-related health guidelines.

ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (EITK)

(Audit Course – I for M.Tech-I Semester)

M. Tech I Semester: Common for all branches						Scheme: 2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
AC103	AC-I	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		2	0	0	0	-	-	-

Course Outcomes:

After the completion of the course students will be able to

CO1: Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change

CO2: Understand the need for protecting traditional knowledge and its significance in the global economy

CO3: Understand the legal framework and policies related to traditional knowledge protection

CO4: Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms

CO5: Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

UNIT – I

Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge - Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge

UNIT – II

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK.

UNIT – III

Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

UNIT – IV

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT – V

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

Textbooks:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. *Introduction to Indian Knowledge System: Concepts and Applications*, PHI Learning Pvt. Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh, *Traditional Knowledge System and*

Technology in India, Pratibha Prakashan 2012.

References:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. *Indian Astronomy: A Source Book*, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. *History of Technology in India*, Vol. I, Indian National Science Academy, New Delhi, 1997
5. Acarya, P.K. *Indian Architecture*, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. *Public Administration in Ancient India,* Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh,*Indian Knowledge Systems Vol – I & II,* Indian Institute of Advanced Study, Shimla, H.P., 2022

Online -Resources:

1. https://www.youtube.com/watch?v=LZP1StpYEPM
2. http://nptel.ac.in/courses/121106003/

CMOS DIGITAL IC DESIGN LAB (CDICD(P))

M. Tech I Semester VLSI & ES						Scheme: 2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC859	PCL	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		0	0	4	2	40	60	100
Sessional Exam Duration:2 Hrs					End Exam Duration:3 Hrs			

Course Outcomes:

After the completion of the course students will be able to

- **CO1**: Explain the VLSI Design Methodologies using any VLSI design tool.
- **CO2**: Grasp the significance of various design logic Circuits in full-custom IC Design
- **CO3**: Explain the Physical Verification in Layout Extraction.
- **CO4**: Fully appreciate the design and analyze of CMOS Digital Circuits
- **CO5:** Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

LIST OF EXPERIMENTS

(Any 12 experiments need to be done)

The students are required to design and implement the Circuit and Layout using CMOS Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS Lab (MDSP(P))

M.Tech I Semester VLSI & ES						Scheme:2025		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
EC860	PCL	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		0	0	4	2	40	60	100
Sessional Exam Duration: 2 Hrs						End Exam Duration: 3Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Install, configure and utilize tool sets for developing applications based on ARM processor core**.**

CO2: Design and develop the ARM7 based embedded systems for various applications**.**

CO3: Develop application programs on ARM and DSP development boards both in assembly and C.

CO4: Design and Implement the digital filters on DSP6713 processor.

CO5: Analyze the hardware and software interaction and integration

LIST OF EXPERIMENTS

Any 12 experiments need to be done, Minimum 02 from Part B

Part A

Experiments to be carried out on Cortex-Mx development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly code and C code to compute Euclidian distance between any two points
13. To develop assembly code and study the impact of parallel, serial and mixed execution
14. To develop assembly and C code for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signal

Software Requirements:

Keil for ARM, Code Composer Studio

Hardware Requirements:

ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit